Higher National Unit Specification

General information for centres

Unit title: Combinational Logic

Unit code: DG3C 34

Unit purpose: This Unit is designed to enable candidates to gain knowledge and understanding and apply basic digital concepts applicable to combinational logic circuits. It provides candidates with an opportunity to develop the knowledge and skills to be able to design and construct combinational logic circuits to meet a design brief.

On completion of the Unit candidates should be able to:

1. Solve problems involving number systems and binary arithmetic.
2. Draw truth tables for common logic gates and derive combinational logic expressions.
3. Interpret TTL and CMOS data sheets and use these devices in digital systems.
4. Design and implement combinational logic circuits.

Credit value: 1 HN Credit at SCQF level 7: (8 SCQF credit points at SCQF level 7*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should have a basic knowledge of digital electronic engineering. This may be evidenced by the possession of Higher Electronics, Intermediate 2 Electronic and Electrical Fundamentals or the following National Qualification Units: E9S3 04 Combinational Logic; and E9SB 12 Logic Families and Digital System Analysis.

Core skills: There may be opportunities to gather evidence towards Core Skills in this Unit, although there is no automatic certification of Core Skills or Core Skills components.

Context for delivery: This Unit was developed for the HNC/D Electronics award. If the Unit is used in another group award it is recommended that it should be taught and assessed within the context of the particular group award to which it contributes.

General information for centres (cont)

Assessment: It is recommended that the assessment for all four Outcomes in this Unit are combined into one assessment paper and a practical exercise. The paper should be taken by candidates at one single assessment event, which should last two hours. The practical design exercise should be no more than three hours but at the discretion of the centre. The assessment paper could be composed of a suitable balance of short answer, restricted response and structured questions. Assessment should be conducted under controlled, supervised conditions. It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

Higher National Unit specification: statement of standards

Unit title: Combinational Logic

Unit code: DG3C 34

The sections of the Unit stating the Outcomes, knowledge and/or skills, and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Solve problems involving number systems and binary arithmetic.

Knowledge and/or skills

- Decimal number system
- Binary and hexadecimal number systems
- Conversion methods between number systems
- Two's complement representation of binary numbers
- Signed binary arithmetic

Evidence requirements

Evidence for the knowledge and/or skills in this Outcome will be provided on a sample basis and be presented in response to specific questions. Each candidate will need to demonstrate that he/she can answer correctly questions based on a sample of the items shown above. In any assessment of this Outcome four out of five knowledge and/or skills should be sampled.

In order to ensure candidates will not be able to foresee the items on which they will be questioned on a different sample of four knowledge and/or skill items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all four items.

When sampling takes place a candidate's response can be judged satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

- write binary and hexadecimal numbers
- convert decimal numbers to binary and vice versa
- convert binary numbers to hexadecimal and vice versa
- perform addition and subtraction using signed binary arithmetic.

Higher National Unit specification: statement of standards (cont)

Unit title: Combinational Logic

Evidence should be generated through assessments undertaken in controlled supervised conditions. Assessments should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or calculators to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of short answer or restricted response questions.

Outcome 2

Draw truth tables for common logic gates and derive combinational logic expressions.

Knowledge and/or skills

- Traditional and ANSI/IEC gate symbols.
- Truth tables and associated Boolean expression for AND/OR/NOT/EXOR/NAND and NOR gates
- Combinational logic expression in sum of products (S of P) and product of sums (P of S) forms
- Implement combinational logic expressions
- Half and full adder full adder circuits

Evidence requirements

Evidence for the knowledge and skills in this Outcome will be provided on a sample basis. The evidence may be presented in response to specific questions. Each candidate will need to demonstrate that he/she can answer questions based on a sample of the above shown items. In any assessment of this Outcome four out of five knowledge and/or skills items should be sampled.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a different sample is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all four items.

When an item is sampled a candidate's response can be judged satisfactory when the evidence meets the requirements of each item by showing that the candidate is able to:

- draw traditional and ANSI/IEC gate symbols
- draw the truth table for each gate
- write the Boolean expression for each gate
- write combinational logic expressions in Sum of Product and Product of Sum forms
- draw circuit diagrams to implement combinational logic expressions

- derive half adder and full adder logic expressions and draw the corresponding circuit diagrams

Assessment guidelines

Evidence of candidate knowledge may take the form of short answer or restricted response questions.

Outcome 3

Interpret TTL and CMOS data sheets and use these devices in digital systems.

Knowledge and/or skills

- Analogue and digital signals
- TTL and CMOS device numbers
- Interpret manufacturers data sheets for logic device characteristics and pin lay out
- Noise margin and noise immunity
- Use of open collector/drain devices
- TTL and CMOS device compatibility
- Interface TTL and CMOS devices
- Select the most appropriate family and device for a particular application

Evidence requirements

Evidence for the knowledge and/or skills in the Outcome will be provided on a sample basis and be presented in response or action to specific questions. Each candidate will need to demonstrate that he/she can correctly answer questions based on a sample of the items shown above. In any assessment of this Outcome six out eight knowledge and/or skills items should be sampled. It is recommended that in any assessment, candidates may be assessed predominantly on CMOS devices where applicable since these are more commonly used by industry.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a different sample of six out of eight knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all 6 items.

When an item is sampled a candidate's response can be judged satisfactory when the evidence is sufficient to meet the requirements for each item by showing that the candidate is able to:

- state whether a given signal is digital or analogue
- interpret data sheets for a number of TTL and CMOS devices and state the type of device and obtain it's characteristics
- explain the concepts of noise margin and noise immunity

- explain the use of open drain/collector devices
- show how a pull up resistor is required to produce HIGH and LOW level signals when using open drain/collector devices
- explain pin compatibility, functionally equivalence and electrical compatibility of TTL and CMOS devices
- explain the interconnection circuit required for a TTL device to drive a CMOS gate
- explain how CMOS device could be interfaced to drive a TTL gate
- explain how a TTL device is interfaced to drive a CMOS gate

Assessment guidelines

A balanced mix of short answer, restricted response and structured questions should be used to elicit candidate evidence.

Outcome 4

Design and implement combinational logic circuits.

Knowledge and/or skills

- Interpret written specifications
- Boolean expressions in sum of product (S of P) and product of sum (P of S) forms.
- Truth tables.
- Logic expression minimisation using Boolean algebra and Karnaugh mapping
- Avoidance of static hazards
- Conversion to NAND/NOR forms using DeMorgan's theorems
- Software check of design
- Design implementation

Evidence requirements

Evidence for the knowledge and skills element of this Outcome will be provided by the candidate demonstrating an understanding of the design process.

In any assessment of the Outcome the candidate should obtain a logic expression which meets the design brief, minimise the expression avoiding static hazards, simulate the circuit and construct a correctly functioning circuit which meets the design specification.

In order to ensure that candidates will not be able to anticipate the content of the written specifications a list of at least six design briefs should be available for assessment use.

Assessment guidelines

The written specifications for each design brief should encompass at least six of the knowledge and skills items specified.

Administrative Information

Unit code: DG3C 34

Unit title: Combinational Logic

Superclass category: XL

Date of publication: May 2004

Version: 02 (July 2005)

Source: SQA

Higher National Unit specification: support notes

Unit title: Combinational Logic

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

The unit has been written in order to allow candidates to develop knowledge, understanding and skills in the following areas:

1. the use of binary arithmetic in digital systems
2. production of simple combinational logic expressions
3. the use of TTL and CMOS logic families
4. design, construction and testing of combinational logic circuits to meet particular applications

This Unit has been developed as part of a group of five digital electronics Units comprising Combinational Logic, Sequential Logic, MSI Devices, Microprocessor and Microcontroller Technology and Programmable Logic Devices. This Unit and Sequential Logic are both at SCQF level 7 and are core Units within the Principles/Technology section of the HNC Electronics award. These two Units plus the MSI Devices and Programmable Logic Devices Units which are SCQF level 8 Units are in the Principles/Technology section of the HND Electronics award. The Microprocessor and Microcontroller Technology Unit is in the options section of the HND Electronics Framework.

The five Units mentioned in the previous paragraph have been developed as an integrated suite of Units to meet the digital electronics requirements of the new HNC/HND Electronics awards. As well as providing a complete course in digital electronics these Units provide important underpinning knowledge and skills for other parts of the HNC/HND awards particularly those relating to computer hardware engineering.

In designing this Unit, the writers have identified the range of topics they would expect lecturers to cover. They have also given recommendations as to how much time should be allocated to each Outcome. This has been done to help tutors to decide the depth of treatment that should be give to each topic within an Outcome. Whilst it is not mandatory for centres to use this list of topics it is strongly recommended that they do so to ensure consistency and continuity of teaching and learning across the digital electronics Units and because the assessment exemplar pack for this Unit is based on the knowledge and/or skills and list of topics in each of the Outcomes.

A list of topics is given below. Lecturers are advised to study this list of topics in conjunction with the assessment exemplar pack so that they can get a clear indication of the standard of achievement expected of candidates in this Unit.

Higher National Unit specification: support notes (cont)

Unit title: Combinational Logic

1. Solve problems involving number systems and binary arithmetic. (5 hours)

Revision of decimal number system
Binary and hexadecimal number systems
Decimal/binary conversion methods
Decimal/hexadecimal conversion methods
Binary/hexadecimal conversion methods
Representation of negative binary numbers and twos complement arithmetic
Signed binary addition and subtraction

2. Draw truth tables for common logic gates and derive combinational logic expressions (6 hours)

Traditional and ANSI/IEE gate symbols for AND/OR/NOT/EXOR/NAND/NOR logic gates
Truth table and Boolean expression for each gate.
Combinational logic expressions in Sum of Product (S of P) and Product of Sums (P of S) forms.
Proof of logic identities using truth tables.
Derivation of Sum and Carry out expressions for a half adder.

Areas for experimental and circuit construction work may include the following:-

Use logic tutor boards to verify logic functions.
Use simulation to verify logic identities.
Use simulation and logic tutor boards to implement logic expressions.
Use simulation and tutor boards to perform binary addition.

3. Interpret TTL and CMOS data sheets and use these devices in digital systems (15 hours)

Compare analogue and digital signals
TTL and CMOS logic families
TTL characteristics for 74LS, 74ALS and 74F devices

Device characteristics: propagation delay, maximum clock frequency, power dissipation, fan out
Voltage parameters: Vcc, V_{OH}min, V_{OL}max, V_{IL}max. noise margin and noise immunity

CMOS characteristics for 74AC/ACT, 74HC/HCT and 74AHC/AHCT

Higher National Unit specification: support notes (cont)

Unit title: Combinational Logic

Device characteristics: propagation delay, power dissipation, fan out

Voltage parameters: Vdd, V_{IH}min, V_{IL}max, V_{OH}min, V_{OL}max
noise margin and noise immunity

Compare TTL and CMOS gate characteristics

CMOS/TTL: pin compatability, functional equivalence, electrical compatibility, Interfacing problems

Characteristics and use of open collector/drain devices

Areas for experimental and circuit construction work may include the following:

Interface incompatible TTL and CMOS devices.

Drive output loads.

4. Design and Implement Combinational Logic Circuits (12 hours)

Laws of Boolean algebra: Absorption A .(A + B) = A

	A + (A . B) = A
Associative	A . (B . C) = (A . B) . C
	A + (B + C) = (A +B) + C
Commutative	A . B = B . A
	A + B = B + A
Distributive	A . (B + C) = A . B + A . C
	A + (B . C) = (A + B) . (A + C)

Hence

A + A = 1	A . A = 0
A . 1 = A	A + 1 = 1

Produce truth tables for 4 input variable combinational logic expressions in sum of product (minterm) and product of sum (maxterm) form.

Minimise expressions using Boolean algebra and Karnaugh mapping.

Design minimised circuits using Karnaugh mapping and avoiding static hazards.

Use DeMorgan's theorems to convert expressions to NAND/NOR forms.

Implement the design.

Areas for experimental and circuit construction work may include the following:

Construct logic circuits to implement logic expressions.
Use logic probes to analyse and fault find circuits
Simulate logic expressions.
Use software to check minimised expressions
Use software to check NAND/NOR conversions.
Use computer software to minimise expressions and check using Karnaugh mapping.
Convert logic expressions to NAND/NOR form using software and check using DeMorgan's theorems.
Hardwire implement logic designs and test for correct operation.

Unit Assessment

Two hour written test having a balanced mix of short answer, restricted response and structured questions designed to elicit evidence of candidate knowledge.

Circuit design and build practical exercise in which the candidate has to interpret a written problem, design a circuit solution, construct and test the circuit. Whilst at the discretion of the centre this exercise should last no more than three hours.

Guidance on the delivery and assessment of this Unit

This Unit is a suitable introduction to digital electronic systems. It is also a suitable lead-in to Sequential Logic

The Unit has been designed to allow candidates sufficient time to carry out a range of practical experimentation, circuit construction and verification exercises to supplement their learning. Tutors should make available experimental exercises which will allow candidates, where possible, to work on their own. Candidates should have free access to manufacturers' data sheets for the devices used. The experimental work carried out as part of this Unit will provide candidates with good practice in experimental techniques in preparation for the Graded Unit.

Computer simulation could form part of the teaching and learning process such as the verification of Boolean identities, Karnaugh mapping and DeMorgan transformations. It could also be used to complement experimental work.

As this Unit provides the core of digital electronics it is recommended that the Unit be delivered towards the start of HNC/HND courses.

Higher National Unit specification: support notes (cont)

Unit title: Combinational Logic

Details on approaches to assessment are given under Evidence requirements and Assessment guidelines under each Outcome in the Higher National Unit specification: statement of standards section. It is recommended that these sections be read carefully before proceeding with assessment of candidates.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of on-line support. Candidates will also require access to a centre which, can provide circuit construction facilities. With regard to assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence. Arrangements would be required to ensure that the evidence whether done at a single or at multiple events was conducted under controlled, supervised conditions.

To keep administration arrangements to a minimum, it is recommended that a single assessment paper (taken by candidates at a single assessment event) be used for distance learning candidates.

For information on normal open learning arrangements, please refer to the SQA guide *Assessment and Quality Assurance of Open and Distance Learning* (SQA 2000)

Special needs

This Unit specification is intended to ensure that there are no artificial barriers to learning or assessment. Special needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments or considering special alternative Outcomes for Units. For information on these, please refer to the SQA document *Guidance on Special Assessment Arrangements* (SQA, 2001).

General information for candidates

Unit title: Combinational Logic

This Unit has been designed to allow you to develop knowledge, understanding and skills associated with combinational logic, which is the basis of digital electronics and underpins more advanced work in this area of study.

The early part of the Unit deals with the basic elements of digital electronics and should provide you with a good grounding in this subject area. For those who have studied digital in an earlier course this Unit will provide an opportunity for revision.

The Unit will enable you to interpret manufacturers data sheets for a range of TTL and CMOS devices and hence provide you with the knowledge to select the most appropriate device for a particular application. On completion of the Unit you should be able to read and draw circuit diagrams containing standard digital devices.

The Unit will also enable you to analyse a problem and write the appropriate logic expression which meets the design requirement. You will also learn to use truth tables, Karnaugh maps and DeMorgan's theorems to produce the most economic design to meet the application requirements.

You will also be able to use computer software to simulate and test your design solution for functional accuracy.

By the end of the Unit you will be expected to design and construct circuits which meet stated design requirements using the minimum number of devices. You should be able to check, using logic measuring equipment, that the circuit meets the design brief.

The final assessment will take the form of a short answer written test paper, lasting two hours, taken under supervised, controlled closed book conditions. You will not be allowed to take notes, textbooks etc into the assessment. You will however have access to device data sheets. In order to allow you to show evidence of practical expertise, there will be a design and construct exercise where you will be expected to design and build a circuit to perform a specified function. This latter exercise is likely to be conducted in a laboratory at a different time from the written assessment and will last no more than three hours.