Higher National Unit Specification

General information for centres

Unit title: Field Programmable Gate Arrays

Unit code: DG3P 35

Unit purpose: This Unit is designed to enable candidates to gain some knowledge and understanding of the architecture and technology used within Field Programmable Gate Arrays and to allow the candidates to develop some of the necessary skills required in using the associated design tools.

On completion of the Unit candidates should be able to:

1. Explain the architecture and technology used within FPGAs.
2. Compare FPGAs with alternative devices.
3. Use FPGA design tools.

Credit value: 1 HN Credit at SCQF level 8: (8 SCQF credit points at SCQF level 8*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should have a basic knowledge and understanding of digital electronics and have some experience in designing combinational logic circuits and synchronous sequential logic circuits using fixed function logic devices. This may be evidenced by possession of the following HN Units Combinational Logic and Sequential Logic.

Core skills: There may be opportunities to gather evidence towards Core Skills in this Unit, although there is no automatic certification of Core Skills or Core Skills components.

Context for delivery: This Unit was developed for the HNC/D Electronics awards. If the Unit is used in another group award(s) it is recommended that it should be taught and assessed within the context of the particular group award(s) to which it contributes.

General information for centres

Assessment: The assessment of Outcome 1 and Outcome 2 in this Unit should be combined together into one assessment paper. This paper should be taken by candidates at one single assessment event, which should last one hour. The assessment paper should be composed of an appropriate balance of short answer, restricted response and structured questions. This assessment should be conducted under controlled, supervised closed book conditions. The assessment of Outcome 3 should be conducted under supervised laboratory conditions. The main design work should be completed within two hours. The assessor should observe the candidates to ensure they are individually able to use the design tools.

Candidates should submit a report containing a hardcopy of appropriate files created during the use of the design tools. The candidates should also be given the opportunity to program and test the device. A further two hours should be allocated to allow this work to be completed. This assessment should be conducted under open book conditions. It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

Higher National Unit specification: statement of standards

Unit title: Field Programmable Gate Arrays

Unit code: DG3P 35

The sections of the Unit stating the Outcomes, knowledge and/or skills and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Explain the architecture and technology used within FPGAs

Knowledge and/or skills

- Basic array structure used within FPGAs
- Different types of configurable logic blocks
- Resources available within typical I/O blocks
- Variety of available routing resources
- Additional resources
- Main technologies used to configure FPGAs

Evidence requirements

Evidence for this Outcome will be collected by response to questions.

The candidate must answer questions to the standard specified below:

- basic array structure used within FPGAs

The basic structure consisting of an array of Configurable Logic Blocks (CLBs) separated by routing channels and surrounded by a perimeter of Input/Output Blocks (IOBs) should be described.

- different types of configurable logic blocks

The two main types of configurable logic block must be described ie those based on Look Up Tables (LUT based) and those based on muliplexers (MUX based).

- resources available within typical I/O blocks

Higher National Unit specification: statement of standards (cont)

Unit title: Field Programmable Gate Arrays

At least three out of the following list of five resources available within typical I/O blocks should be explained: flip-flops/latches; tri-state buffers; slew rate control; passive pull-up/pull-down; delay paths.

- variety of available routing resources

At least two different routing resources from the following list should be explained: direct interconnect; general purpose interconnect using switch matrices; horizontal and vertical longlines.

- additional resources

At least three different additional resources from the following list should be explained: global clock buffers; tri-state buffers for busses; global set/reset; internal oscillator; memory blocks; embedded processors.

- main technologies used to configure FPGAs

The two main technologies used to configure FPGAs should be explained. i.e. SRAM and Antifuse. At least one advantage for each type should be included in the explanation.

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment for this Outcome may be combined with Outcome 2 to form a single assessment paper.

Outcome 2

Compare FPGAs with alternative devices.

Knowledge and/or skills

- Advantages of using programmable logic as an alternative to fixed function devices
- Advantages and disadvantages of using FPGAs compared to other types of customisable devices

Higher National Unit specification: statement of standards (cont)

Unit title: Field Programmable Gate Arrays

Evidence requirements

Evidence for this Outcome will be collected by response to questions.

The candidate must answer questions to the standard specified below:

- advantages of using programmable logic as an alternative to fixed function devices

At least three of the following six factors should be considered: costs; speed; power consumption; reliability; flexibility; security

- advantages and disadvantages of using FPGAs compared to other types of customisable devices

At least one other customisable device from the following list must be compared: full custom, standard cell, mask programmable gate arrays, programmable logic devices.
The candidate should not know in advance which alternate device will be compared.
At least three of the following four factors must be included in the comparison: costs, density, performance, time to market.

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment for this Outcome may be combined with Outcome 1 to form a single assessment paper.

Outcome 3

Use FPGA design tools.

Knowledge and/or skills

- Enter circuit design using appropriate data entry methods
- Simulate design
- Use synthesis tools
- Use place and route tools
- Use timing analysis tools
- Program and test device

Higher National Unit specification: statement of standards (cont)

Unit title: Field Programmable Gate Arrays

Evidence requirements

Evidence for this Outcome will be collected by response to a practical assignment. The assignment must involve the design of a circuit containing at least three different functional blocks on the top level of hierarchy. At least one of the blocks must involve synchronous sequential logic. Also, at least one of the blocks must contain at least two levels of hierarchy.

The design entry methods should involve both schematic capture and the use of a hardware description language such as VHDL.

Evidence should be generated through assessment undertaken in supervised laboratory conditions. The assessor should observe the candidates to ensure they are individually able to use the design tools. Candidates should submit a report containing a hardcopy of appropriate files created during the use of the design tools. The candidates should also be given the opportunity to programme and test the device. The assessment may be conducted under open book conditions and as such candidates should be allowed to refer to any textbooks, handouts or notes during the assessment.

Assessment guidelines

As an aid to ensuring the authenticity of the submissions candidates may be issued similar but different design specifications.

Administrative Information

Unit code: DG3P 35

Unit title: Field Programmable Gate Arrays

Superclass category: XL

Date of publication: May 2004

Version: 01

Source: SQA

Higher National Unit specification: support notes

Unit title: Field Programmable Gate Arrays

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

This Unit has been written in order to allow candidates to develop knowledge, understanding and skills related to the use Field Programmable Gate Arrays. A comparison is also made between FPGAs and alternative devices.

In designing this Unit the Unit writers have identified the range and depth of material they would expect lecturers to cover. They have also given recommendations as to how much time should be allocated to each Outcome. This has been done to help tutors to decide what depth of treatment should be given to the topics attached to each of the Outcomes. Centres should not feel limited by the suggested approach and may wish to add material to suit local requirements and resources. However it is strongly recommended that as a minimum the following material should be covered to ensure continuity of teaching and learning.

The following material is designed to give guidance on the coverage required for each Outcome.

Outcome 1
Explain the architecture and technology used within FPGAs (5 hours)

A Field Programmable Gate Array (FPGA) consists of an array of configurable logic blocks which can be interconnected using programmable routing channels. The device will also contain configurable input/output blocks which allow connection to the external pins. Unlike PLDs, FPGAs allow multiple levels of logic and since path lengths can vary, accurate timing analysis can only by performed after the design has been placed and routed. Although the detailed complexity varies from one manufacturer to another most of the logic block architectures are either Look up Table (LUT) based or Multiplexer (MUX) based. Look Up Tables are basically RAM type memory blocks used within the configurable logic blocks as function generators. A typical 4 bit LUT can implement any function of 4 variables in 'sum of minterm' form. The configurable logic blocks may contain a combination of LUTs so that larger functions can be implemented. Registers may also be included so that synchronous sequential logic can be implemented. Obviously, it is also possible to use the LUTs as RAM for the purpose of storing data although many FPGAs provide dedicated RAM blocks for this purpose.

Multiplexers can also be used to implement logic functions by connecting the function variables and an appropriate combination of 0s and 1s to the multiplexer data and select inputs. Typical logic modules may contain a combination of muliplexers and basic gates. Registers may also be included. Generally the MUX based logic blocks are smaller and

contain less logic than LUT based blocks and therefore tend to involve more routing between blocks to create larger functions.

The configurable logic blocks within FPGAs generally contain less combinational logic than the function blocks within complex PLDs. However, there are many more of them and since each CLB may also contain one or two flip-flops, FPGAs are particularly suitable for 'register rich' applications. I/O blocks support input, output, bi-directional, and tri-state modes. I/O blocks may also contain registers and latches. Programmable delay paths may be included to allow control over setup and hold times. Outputs buffers may also allow control over slew rate to reduce noise in signals that do not require high speed. Internal resistors may also be provided to allow passive pull-up or pull-down of inputs.

Different types of routing resources are provided within an FPGA. Direct interconnect between adjacent CLBs or CLBs and IOBs is used for high speed signals between adjacent blocks. General purpose interconnect is created using short lines which intersect at switch matrices between the CLBs. The switch matrices allow signals to be routed from any channel approaching an intersection to any other channel leaving it. Longlines are typically used for high fan-out signals such as clock signals or, in conjunction with tri-state buffers, to provide internal bus systems. Additional resources include global buffers which can be used to reduce skew and provide high fan-out capability for signals such as clocks. A global set/reset facility may be used to initialise all internal flip/flops during power-up, re-configuration or in response to an external signal. The internal oscillator, normally used during the configuration process in SRAM based FPGAs, may also be used as part of the circuit after configuration. This can remove the need for an external clock generator.

The two main technologies used by different manufacturers to configure FPGAs are 'SRAM' and 'antifuse'. SRAM uses static RAM cells to store the configuration. SRAM cells are volatile and lose the data stored in them when the power is removed. Therefore, FPGAs based on SRAM technology must be configured each time they are powered up. The configuration data may be supplied from an external PROM or a host processor. Antifuse technology is similar to fuse technology except that the links are normally open and are made to conduct by a high programming voltage causing breakdown of the insulating layer within the antifuse. Like fuses the effect is irreversible and hence FPGAs based on antifuse technology are 'One Time Programmable'. However they are non-volatile and do not require to be reconfigured on power up. A higher density of interconnections is possible using antifuse technology due to the relatively larger size of the SRAM cells (typically 6 transistors). Therefore, antifuse based FPGAs tend to have more abundant routing resources than SRAM based FPGAs. The antifuse, when made to conduct, also has a lower resistance and less capacitance than the pass transistors used in SRAM cells which tends to increase speed and reduce power consumption.

However, SRAM technology has the advantage of allowing the possibility of 'In Circuit Reconfigurability' (ICR). Systems can be updated using the same FPGA by simply changing the configuration data. It is also possible to reconfigure the FPGA to perform different tasks at different times within the system. This is known as ‘dynamic reconfiguration’ and

theoretically can lead to ‘greater than 100% utilisation’. Applications making use of 'partial dynamic reconfiguration' where only a part of the FPGAs is reconfigured while the rest remains fully functional are also possible with some SRAM based FPGAs.

These techniques open up the possibility of 'reconfigurable computing' where tasks normally performed by microprocessors could be performed by dedicated circuits, at much higher speeds, which are configured within FPGAs as required. The larger FPGAs now include embedded processors to allow complete computing systems involving dedicated processors to be implemented within a single FPGA.

Outcome 2
Compare FPGAs with alternative devices. (5 hours)

In general, FPGAs have all the same advantages as PLDs over fixed logic devices in terms of reducing costs, board size and power consumption as well as increasing speed, flexibility, reliability and security. However the larger size and complexity of FPGAs allow complete systems to be implemented within a single FPGA.

Compared with standard fixed function devices, FPGAs offer the following advantages:

- reduced cost:
  since FPGAs are capable of replacing many fixed function ICs, the ‘chip count’ and board size can be greatly reduced, thereby reducing manufacturing and inventory costs.
- reduced power consumption:
  fewer ICs tend to require less power. This can also lead to the feasibility of making systems battery powered and therefore more portable
- increased speed:
  reducing the physical size of a circuit tends to reduce time delays and therefore the maximum frequency of signals can be increased
- increased reliability:
  since more of the circuit is implemented internally within FPGAs there are fewer external connections which are often the cause of faults
- increased flexibility:
  FPGAs offer the designer greater freedom in the way a design can be implemented instead of being constrained by the features available on standard ICs. In addition, design changes can often be implemented within the FPGA without having to make changes to the board

- increased security:
  since the circuit is effectively hidden within the FPGA it is more difficult for the design to be copied

In order to allow comparison with alternative customisable devices a brief introduction to each type must be covered.

Full Custom devices are designed from 'scratch'. The designer has complete freedom, within the design rules, to place the different components (transistors, resistors, etc.) anywhere within the chip area and interconnect them as required. This usually results in the most efficient implementation of the design with the best performance and minimum chip area. It is also possible to implement both analogue and digital circuits on the same IC.

However, every mask used in the photolithography stages of the fabrication process must be customised for the particular IC. The initial time, effort and specialist skills required for this means that the NRE (non recurring engineering) costs can be quite high. Hence, full custom can only be justified for applications involving high volume production otherwise the unit cost would be too high.

Standard Cell devices are similar to full custom in that every mask in the fabrication process is customised for the particular IC. However, the designer selects functions from a library of commonly used building blocks or 'standard cells' which have already been designed and optimised. This considerably reduces the design time and initial costs. The cells can be placed anywhere on the chip and then interconnected. A small amount of full custom design may be required to finish the circuit. As with full custom, the chip size is not pre-defined and only components actually required by the circuit are fabricated.. However, the circuit density and performance are usually less than can be achieved with full custom. Reasonably high volume production is still required to justify the initial costs.

In Mask Programmable Gate Arrays, all the components have already been fabricated on the chip, leaving only the final metalisation layers to decide how they are to be interconnected. Since most of the fabrication is fixed, gate arrays can be made in large quantities up to the point before they are committed to particular designs. Only the final metalisation masks have to be customised. This reduces the initial cost compared with standard cell. However, the user still has to rely on a chip manufacture to finish the fabrication process.

The layout usually consists of rows of cells containing basic components with routing channels left between the rows. The components within each cell can be interconnected to form logic functions. The cells can then be interconnected to form the final circuit. Note that, unlike standard cell, the chip size in gate arrays is pre-determined and it is extremely unlikely that all of the fabricated components will be used in the final circuit.

Gate arrays can be cost effective for much lower production volumes than full custom and standard cell.

Higher National Unit specification: support notes (cont)

Unit title: Field Programmable Gate Arrays

Programmable Logic Devices have a rather restrictive architecture based on ‘two level logic’ and basically consist of an array of AND gates connected to an array of OR gates. Although both arrays may be programmable some types of PLD only have one of the arrays programmable. Output cells may contain internal registers allowing the possibility of implementing synchronous sequential logic within the PLD. ‘Complex PLDs’ can be produced by combining a number of simple PLDs within a single device. However, they are generally smaller in capacity and have less flexibility compared to FPGAs.

FPGAs are now of a size where they can compete with mask programmed gate arrays, standard cell or even full custom devices. Although these devices may offer superior performance in terms of speed or power consumption, the savings in time and initial costs make FPGAs an attractive alternative with considerably less risks attached especially compared to standard cell or full custom devices. The reduced 'time to market' through using FPGAs can be a significant advantage. In addition, the SRAM based FPGAs offer features due to their reconfigurability which are not possible with other devices.

Outcome 3
Use FPGA design tools (25 hours)

It is recognised that the specific resources available will vary between centres. However, most FPGA design tools have similar features and design flow. The design is entered using schematic capture or a hardware description language or both. Standard hardware description languages exist such as VHDL or Verilog. Synthesis tools are used to convert the hardware description into the required circuit. Functional simulation can be performed at an early stage. The design is mapped into the architecture and resources available within the target FPGA. Place and route tools are used to fit the circuit into specific CLBs and IOBs within the target FPGA using the appropriate routing resources. The designer can specify timing and placement constraints. A bitstream file is generated for configuration of the FPGA. Static timing analysis tools can be used to determine propagation delays and maximum frequencies. A full timing simulation can be performed to check for glitches.

Unit Assessment
1 hour single assessment paper for Outcomes 1 and 2, plus a 4 hour single practical assessment for Outcome 3

Guidance on the delivery and assessment of this Unit

In addition to covering the generic architectural and technological features of FPGAs it is recommended that candidates be given data on various specific FPGAs from different manufacturers. Candidates may be referred to relevant web sites to gather information on different FPGAs and alternative devices.

A number of practice sessions should be provided to allow candidates to become familiar with the design tools and the standard required for assessment. The candidates should clearly understand the typical design flow. The use of an FPGA editor showing the internal structure of the device may be useful.

Due to the complexity of standard hardware description languages such as VHDL and the limited time available, candidates should not be expected to learn much more than the basic language constructs required to complete the practical assessment. However, they should understand the main concepts within hardware description languages such as concurrency, timing and hierarchy. The difference between structural and behavioural descriptions should also be covered.

It may be beneficial to assess Outcomes 1 and 2 after the practical work in Outcome 3 to allow candidates to relate theory to practice.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of on-line support. Candidates will also require access to suitable design tools. With regard to assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence. Arrangements would be required to ensure that the assessment was conducted under controlled, supervised conditions.

For information on normal open learning arrangements, please refer to the SQA guide *Assessment and Quality of Open and Distance Learning* (SQA 2000).

Special needs

This Unit specification is intended to ensure that there are no artificial barriers to learning or assessment. Special needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments or considering special alternative Outcomes for Units. For information on these, please refer to the SQA document *Guidance on Special Assessment Arrangements* (SQA, 2001).

General information for candidates

Unit title: Field Programmable Gate Arrays

This Unit has been designed to allow you to gain knowledge, understanding and skills related to the use of Field Programmable Gate Arrays. These devices can be 'programmed' or configured to implement large digital circuits within a single device. This technology offers many advantages over standard fixed function integrated circuits and other alternatives.

Outcome 1 of this Unit will provide you with the opportunity to learn about the internal architecture and features of FPGAs and the technologies used to configure them. In Outcome 2, FPGAs are compared with alternative devices. In addition to comparing FPGAs with fixed function devices the comparison will also include other devices that can be configured or customised to some extent by the user. The main factors affecting choice of device will be considered. These two Outcomes will be assessed by a single assessment paper lasting one hour. The precise form of the assessment will depend on the centre providing the Unit. Please ask your lecturer what form the assessment will take. However the assessment will be conducted under controlled, supervised conditions and will be closed book in that you will not be allowed to take notes, textbooks etc. into the assessment.

Designing with FPGAs involves the use of computer software tools capable of allowing the design to be entered, simulated and implemented by producing the data required to configure the chosen FPGA. In Outcome 3 you will be given practical experience in the use of typical FPGA design tools. The particular tools used will depend on the resources available to the centre providing the Unit. The assessment of this Outcome will consist of a practical assignment conducted under supervised laboratory conditions and will be open book in that you will be allowed to refer to notes, etc. during the assessment. The main design work should be completed within two hours. You will be required to produce a report containing prints of the relevant files created using the design tools. You will also be required to program and test the device to show that it meets the given specification. A further two hours will be allocated to allow this work to be completed.