Higher National Unit Specification

General information for centres

Unit title: Programmable Logic Devices

Unit code: DG52 35

Unit purpose: This Unit is designed to enable candidates to gain some knowledge and understanding of the principles and benefits of using programmable logic devices compared to alternatives and to allow the candidates to develop some of the necessary skills required in using the associated design tools.

On completion of this Unit the candidate should be able to:

1. Explain the architecture and technology used within PLDs.
2. Compare PLDs with alternative devices.
3. Use PLD design tools.

Credit value: 1 HN Credit at SCQF level 8: (8 SCQF credit points at SCQF level 8*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should have a basic knowledge and understanding of digital electronics and have some experience in designing combinational logic circuits and synchronous sequential logic circuits using fixed function logic devices. This may be evidenced by possession of the following HN Units Combinational Logic and Sequential Logic.

Core skills: There may be opportunities to gather evidence towards Core Skills in this Unit, although there is no automatic certification of Core Skills or Core Skills components.

Context for delivery: This Unit was developed for the HNC/D Electronics awards. If this Unit is used in another group award(s) it is recommended that it should be taught and assessed within the context of the particular group award(s) to which it contributes.

General information for centres (cont)

Assessment: The assessments for Outcome 1 and Outcome 2 in this Unit should be combined together into one assessment paper. This paper should be taken by candidates at one single assessment event, which should last one hour. The assessment paper should be composed of an appropriate balance of short answer, restricted response and structured questions. This assessment should be conducted under controlled, supervised closed book conditions. The assessment of Outcome 3 should be conducted under supervised laboratory conditions. The main design work should be completed within two hours. The assessor should observe the candidates to ensure they are individually able to use the design tools.

Candidates should submit a report containing a hardcopy of appropriate files created during the use of the design tools. The candidates should also be given the opportunity to program and test the device. A further two hours may be allocated to allow this work to be completed. This assessment may be conducted under open book conditions. It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

Higher National Unit specification: statement of standards

Unit title: Programmable Logic Devices

Unit code: DG52 35

The sections of the Unit stating the Outcomes, knowledge and/or skills, and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Explain the architecture and technology used within PLDs

Knowledge and/or skills

- Basic array structure and degree of programmability used within simple PLDs
- Various technologies used to create programmable links
- Additional features available within PLDs containing programmable output cells
- Difference between SPLDs and CPLDs

Evidence requirements

Evidence for this Outcome will be collected by response to questions.
The candidate must answer questions to the standard specified below:

- basic array structure and degree of programmability used within simple PLDs

  The basic 2 level logic structure composed of an AND array followed by an OR array as used in simple PLDs should be defined. The degree of programmability should be identified for each of the three basic architectural types which all SPLDs are based on i.e. PROM, PLA and PAL. At least one advantage or one disadvantage for each type should be explained.

- various technologies used to create programmable links

  Three main types of programmable link must be defined. i.e. fuse, UV erasable and electrically erasable. At least one advantage or one disadvantage of each technology must be explained.

- additional features available within PLDs containing programmable output cells

Higher National Unit specification: statement of standards (cont)

Unit title: Programmable Logic Devices

At least three out of the following list of five additional features must be explained: programmable polarity; registered outputs; tri-state buffers; internal feedback; bi-directional pins

- difference between SPLDs and CPLDs

  The use of an internal global switch matrix to interconnect multiple simple PLD architectures to form complex PLDs should be explained.

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment for this Outcome should be combined with Outcome 2 to form a single assessment paper, details of which are given under Outcome 2

Outcome 2

Compare PLDs with alternative devices

Knowledge and/or skills

- Advantages of using programmable logic as an alternative to fixed function devices
- Advantages and disadvantages of using PLDs compared to other types of customisable devices

Evidence requirements

Evidence for this Outcome will be collected by response to questions.
The candidate must answer questions to the standard specified below:

- advantages of using programmable logic as an alternative to fixed function devices

  At least three of the following six factors should be considered: costs; speed; power consumption; reliability; flexibility; security

- advantages and disadvantages of using PLDs compared to other types of customisable devices

At least one other customisable device from the following list must be compared: full custom, standard cell, mask programmable gate arrays, field programmable gate arrays.

The candidate should not know in advance which alternate device will be compared. At least three of the following four factors must be included in the comparison: costs, density, performance, time to market.

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment for this Outcome should be combined with Outcome 1 to form a single assessment paper. This single assessment paper should be taken at a single assessment event and carried out under supervised, controlled conditions.

Outcome 3

Use PLD design tools

Knowledge and/or skills

- Enter circuit design using appropriate data entry methods
- Simulate design
- Create test vectors
- Enter selected device information
- Create programming file
- Program and test device

Evidence requirements

Evidence for this Outcome will be collected by response to a practical assignment. The assignment must involve the design of a circuit containing at least two functional blocks, one of which must involve synchronous sequential logic.

At least one of the following data entry methods should be used for the sequential logic block: schematic capture, boolean equations, finite state machine syntax.

Truth tables may also be used for the second functional block if it is purely combinational.

Evidence should be generated through assessment undertaken in supervised laboratory conditions. The assessor should observe the candidates to ensure they are individually able to use the design tools. Candidates should submit a report containing a hardcopy of appropriate files created during the use of the design tools. The candidates should also be given the opportunity to program and test the device. The assessment may be conducted under open book conditions and as such candidates should be allowed to refer to any textbooks, handouts or notes during the assessment.

Assessment guidelines

As an aid to ensuring the authenticity of the submissions candidates may be issued similar but different design specifications.

Administrative Information

Unit code: DG52 35

Unit title: Programmable Logic Devices

Superclass category: XL

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Source: SQA

Higher National Unit specification: support notes

Unit title: Programmable Logic Devices

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

This Unit has been written in order to allow candidates to develop knowledge, understanding and skills related to the use of Programmable Logic Devices. A comparison is also made between PLDs and alternative devices.

This Unit has been developed as part of a group of five digital electronics Units comprising Combinational Logic, Sequential Logic, MSI Devices and Programmable Logic Devices and Microprocessor and Microcontroller Technology. Combinational Logic and Sequential Logic are both at SCQF level 7 and are core Units within the Principles and Technology section of the new HNC Electronics award. The MSI Devices and Programmable Logic Devices Units which are SCQF level 8 Units form part of the Principles and Technology section of the new HND Electronics award. The Microprocessor and Microcontroller Technology Unit (SCQF Level 8) is contained within the optional section of the HND Electronics award.

The four Units mentioned in the previous paragraph have been developed as an integrated suite of Units to meet the digital electronics requirements of the new HNC/HND Electronics awards. As well as providing a complete course in digital electronics these Units provide important underpinning knowledge and skills for other parts of the HNC/HND awards particularly those relating to computer hardware engineering.

In designing this Unit the Unit writers have identified the range and depth of material they would expect lecturers to cover. They have also given recommendations as to how much time should be allocated to each Outcome. This has been done to help tutors to decide what depth of treatment should be given to the topics attached to each of the Outcomes. Centres should not feel limited by the suggested approach and may wish to add material to suit local requirements and resources. However it is strongly recommended that as a minimum the following material be covered to ensure continuity of teaching and learning and because the assessment exemplar pack for this Unit is based on the knowledge and/or skills and topics in each of the Outcomes.

The following material is designed to give guidance on the coverage required for each Outcome.

Higher National Unit specification: support notes (cont)

Unit title: Programmable Logic Devices

Outcome 1
Explain the architecture and technology used within PLDs (5 hours)

PLD architecture makes use of the fact that any logic function can be implemented in sum of product form using only two levels of logic. Hence the basic architecture consists of an array of AND gates followed by an array of OR gates. The degree of programmability therefore extends to three possibilities:

- fixed AND, programmable OR (i.e. PROM like devices)
- programmable AND, fixed OR (i.e. PAL like devices)
- programmable AND, programmable OR (i.e. PLA like devices)

The candidates should be made aware that although there are many different names used by different manufacturers of PLDs, most are simply a derivative of one of the three basic types. (e.g. GALs are PAL like in basic architecture)

The advantages and disadvantages of each type should relate to factors such as flexibility (e.g. PLAs allow the possibility of 'product sharing' since the OR array is also programmable), efficiency (e.g. PROMS tend to have a large number of unused AND gates in most applications and also require equations to be implemented in 'sum of minterm' form), speed and power consumption (e.g. since only one array is programmable PALs tend to be faster and consume less power than PLAs and, although not as versatile as PLAs, may be considered a good compromise.)

Only a brief explanation of each of the technologies used to produce programmable links is required. The programmable links may be fuse type, UV erasable or electrically erasable. In the fuse type the circuit is created by blowing tiny fuses where links are not wanted and leaving the rest intact. This is a permanent and irreversible process and obviously the programmability of these devices cannot be fully tested by the PLD manufacturer. Erasable PLDs use links based on charge storage. This means that they can be erased by removing the charge electrically or by exposure to UV light. UV types require a more expensive ceramic package with a quartz window to allow the light to enter. Exposure times are approximately 15 minutes. Electrically erasable types can be erased almost immediately and can be supplied in economical plastic packages. Erasable devices obviously have the advantage of being reusable and are completely testable. However they can suffer from charge leakage over a long period of time and may eventually lose their configuration.

Only a brief explanation of the various additional features found in PLD output cells is required. Many PLDs have built in bistables and feedback paths. This allows sequential logic to be implemented within the PLD. Feedback paths can also be used to build larger combinational logic functions than can be accommodated in a single output. Tri-state buffers may be included in the PLD output cells to allow connection to bus systems. Tri-state buffers may also be used in conjunction with feedback paths to allow the possibility of bi-directional pins. Another additional feature often found in PLD output cells is the ability to program the polarity of the logic functions. The logic can be made 'active high' or 'active low' using programmable inverters in the output cells. These commonly make use of exclusive OR gates with a programmable link to ground on one of the inputs. In applications where the inverse of the required function contains less product terms, programmable polarity can be used to allow the inverse function to be implemented within the arrays and then inverted to produce the required function at the device output pin.

Complex PLDs (CPLDs) basically combine a number of simple PLD structures into one device by using a programmable switch matrix. However, since the connectivity within the switch matrix may be limited it may not always be possible to route every signal between structural blocks. Typical CPLDs have at least four PAL like structures within the one device.

Outcome 2
Compare PLDs with alternative devices (5 hours)

Compared with standard fixed function devices, PLDs offer the following advantages:

- reduced cost:
  since PLDs are capable of replacing many fixed function ICs, the 'chip count' and board size can be greatly reduced, thereby reducing manufacturing and inventory costs

- reduced power consumption:
  fewer ICs tend to require less power. This can also lead to the feasibility of making systems battery powered and therefore more portable

- increased speed:
  reducing the physical size of a circuit tends to reduce time delays and therefore the maximum frequency of signals can be increased

- increased reliability:
  since more of the circuit is implemented internally within PLDs there are fewer external connections which are often the cause of faults

- increased flexibility:
  PLDs offer the designer greater freedom in the way a design can be implemented instead of being constrained by the features available on standard ICs. In addition, design changes can often be implemented within the PLD without having to make changes to the board

- increased security:
  since the circuit is effectively hidden within the PLD it is more difficult for the design to be copied. Many PLDs provide a security bit feature

In order to allow comparison with alternative customisable devices a brief introduction to each type must be covered.

Full Custom devices are designed from 'scratch'. The designer has complete freedom, within the design rules, to place the different components (transistors, resistors, etc.) anywhere within the chip area and interconnect them as required. This usually results in the most efficient implementation of the design with the best performance and minimum chip area. It is also possible to implement both analogue and digital circuits on the same IC.

However, every mask used in the photolithography stages of the fabrication process must be customised for the particular IC. The initial time, effort and specialist skills required for this means that the NRE (non recurring engineering) costs can be quite high. Hence, full custom can only be justified for applications involving high volume production otherwise the unit cost would be too high.

Standard Cell devices are similar to full custom in that every mask in the fabrication process is customised for the particular IC. However, the designer selects functions from a library of commonly used building blocks or 'standard cells' which have already been designed and optimised. This considerably reduces the design time and initial costs. The cells can be placed anywhere on the chip and then interconnected. A small amount of full custom design may be required to finish the circuit. As with full custom, the chip size is not pre-defined and only components actually required by the circuit are fabricated. However, the circuit density and performance are usually less than can be achieved with full custom. Reasonably high volume production is still required to justify the initial costs.

In Mask Programmable Gate Arrays, all the components have already been fabricated on the chip, leaving only the final metalisation layers to decide how they are to be interconnected. Since most of the fabrication is fixed, gate arrays can be made in large quantities up to the point before they are committed to particular designs. Only the final metalisation masks have to be customised. This reduces the initial cost compared with standard cell. However, the user still has to rely on a chip manufacture to finish the fabrication process.

The layout usually consists of rows of cells containing basic components with routing channels left between the rows. The components within each cell can be interconnected to form logic functions. The cells can then be interconnected to form the final circuit. Note that, unlike standard cell, the chip size in gate arrays is pre-determined and it is extremely unlikely that all of the fabricated components will be used in the final circuit.

Gate arrays can be cost effective for much lower production volumes than full custom and standard cell.

Field Programmable Gate Arrays (FPGAs) are similar in architecture to mask programmable gate arrays except that the user can programme or configure them using programmable links within the array. Also the logic cells in FPGAs are usually more complex than Mask Programmable Gate Arrays. Some FPGAs use SRAM technology to control the links and are therefore volatile i.e. the design is lost when the device is switched off and has to be reloaded on power up. Others use anti-fuse technology which is non-volatile.

All of these devices are generally more complex than PLDs allowing much larger circuits to be implemented. Unlike PLDs they all allow multiple levels of logic. As a result, delays can only be calculated after the circuit has been finally placed and routed. Hence more careful timing analysis and simulation will be required. With the exception of FPGAs, they all require wafer fabrication facilities to complete the design. All of the alternative devices will tend to outperform PLDs with regard to circuit density, overall speed and power consumption. However, due to the low NRE costs and short design time PLDs are particularly suited to smaller designs with low volume production and fast time to market.

Outcome 3
Use PLD design tools (25 hours)

It is recognised that the specific resources available will vary between centres. However, most PLD design tools have similar features and design flow. A design file is created containing a graphical or text based description of the required circuit. The design is checked for syntax errors. The logic is optimised and a simulation model created. Simulation is performed to verify functionality of the design. Test vectors are created. Device information and pin allocation are entered. A file containing the data required to program the device is created. This will normally be in standard JEDEC format. Documentation files may also be created. The programming file is used to program the device using suitable equipment. The device may be tested using test vectors included in the JEDEC file or on a separate test board.

Unit Assessment
A 1 hour single assessment paper for Outcomes 1 and 2, plus a 4 hour single practical assessment for Outcome 3.

Higher National Unit specification: support notes (cont)

Unit title: Programmable Logic Devices

Guidance on the delivery and assessment of this Unit

In addition to covering the generic architectural and technological features of PLDs it is recommended that candidates be given data on various specific PLDs from different manufacturers. Candidates may be referred to relevant web sites to gather information on different PLDs and alternative devices.

Manual completion of simple fuse maps may be a useful educational exercise although it should be noted that it is unlikely that candidates would require this skill in practice, due to the availability of design software.

A number of practice sessions should be provided to allow students to become familiar with the design tools and the standard required for assessment. A review of combinational logic and sequential logic design techniques (state diagrams, etc) may be required. The candidates should clearly understand the typical design flow. Ideally a variety of data entry methods should be tried and compared although this may be limited by time and resources. It may be useful to examine the contents of a JEDEC file containing programming information and standard test vector characters.

The standard of design required for assessment should involve synchronous sequential logic and at least two functional blocks. The ability to combine different functional blocks within a single device is a particular advantage of PLDs compared to standard fixed function devices.

It may be beneficial to assess Outcomes 1 and 2 after the practical work in Outcome 3 to allow candidates to relate theory to practice.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of on-line support. Candidates will also require access to suitable design tools. With regard to assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence. Arrangements would be required to ensure that the evidence whether done at a single or at multiple events was conducted under controlled, supervised conditions.

For information on normal open learning arrangements, please refer to the SQA guide *Assessment and Quality of Open and Distance Learning* (SQA 2000).

Higher National Unit specification: support notes (cont)

Unit title: Programmable Logic Devices

Special needs

This Unit specification is intended to ensure that there are no artificial barriers to learning or assessment. Special needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments or considering special alternative Outcomes for Units. For information on these, please refer to the SQA document *Guidance on Special Assessment Arrangements* (SQA, 2001).

General information for candidates

Unit title: Programmable Logic Devices

This Unit has been designed to allow you to gain knowledge, understanding and skills related to the use of Programmable Logic Devices. These devices can be used to implement combinational and sequential logic circuits internally by making use of programmable links. This technology offers many advantages over standard fixed function integrated circuits.

Outcome 1 of this Unit will provide you with the opportunity to learn about the internal architecture and features of PLDs and the technologies used to produce the programmable links. In Outcome 2, PLDs are compared with alternative devices. In addition to comparing PLDs with fixed function devices the comparison will also include other devices that can be configured or customised to some extent by the user. The main factors affecting choice of device will be considered. These two Outcomes will be assessed in a single assessment paper lasting one hour. The precise form of the assessment will depend on the centre providing the Unit. Please ask your lecturer what form the assessment will take. However the assessment will be conducted under controlled, supervised conditions and will be closed book i.e. you will not be allowed to take notes, textbooks etc. into the assessment.

Designing with PLDs usually involves the use of computer software tools capable of allowing the design to be entered, simulated and implemented by determining the required links. A PLD programmer capable of creating the pattern of links within the device will also be required. PLD programmers can also be used to test the device using instructions known as 'test vectors'. In Outcome 3 you will be given practical experience in the use of typical PLD design tools. The particular tools used will depend on the resources available to the centre providing the Unit. The assessment of this Outcome will consist of a practical assignment conducted under supervised laboratory conditions and will be open book i.e. you will be allowed to refer to notes, etc. during the assessment. The main design work should be completed within two hours. You will be required to produce a report containing prints of the relevant files created using the design tools. You will also be required to program and test the device to show that it meets the given specification. A further two hours will be allocated to allow this work to be completed.