Higher National Unit Specification

General Information for Centres

Unit title: Computer Architecture 1

Unit Code: DH2T 34

Unit purpose: This Unit is designed to develop broad general knowledge and understanding of the theoretical concepts, principles, boundaries and scope of the mechanisms that underpin the use of digital computers. This includes the way in which the internal representation used within the machine can be translated to give human readable values. Study of the Unit also provides a foundation knowledge of the mechanisms used by a processor to communicate with memory and external devices, how a processor deals with requests from external sources, and the characteristics and requirements of the devices that processors can be regularly expected to deal with. The study of the Unit will be of particular benefit to those who wish to undertake further study in the fields of computer programming, providing technical support to other users or new media production.

On completion of this Unit the candidate should be able to:

1. Demonstrate an ability to manipulate and translate data representations.
2. Demonstrate an understanding of the functions of computer system components.
3. Demonstrate an understanding of the principles of Central Processor Unit (CPU) operation.

Credit Value: 1 HN Credit at SCQF level 7: (8 SCQF credit points at SCQF level 7)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

Recommended Prior Knowledge and Skills: Access to this Unit will be at the discretion of the Centre, however it is recommended that candidates should have some prior knowledge and skill in Computing/IT demonstrated by achievement of relevant National Courses or Units at Intermediate 2 or Higher, or appropriate work experience.

For core skills it would be beneficial if candidates had some numeracy skills. This could be demonstrated by the achievement of the core skill components Using Number and/or Using Graphical Information at Intermediate 1 level or equivalent.

Core skills: This Unit gives automatic certification of the following core skill:

Numeracy at Intermediate 2

General Information for Centres

Context of Delivery: If this Unit is delivered as part of a group award, it is recommended that it should be taught and assessed within the group award to which it contributes.

Assessment: When assessing this Unit, it should be borne in mind that many of the concepts are related, and advantage should be taken of this fact for the purposes of assessment. A practical example of related concepts is the need to perform base conversions when calculating addresses when installing hardware. Outcome 1 will be assessed by 20 multiple-choice questions testing knowledge and/or skills and should be conducted as a closed book assessment under supervised conditions. Outcomes 2 and 3 should be open book under supervised conditions and these may be integrated into one holistic assessment.

Some of the evidence requirements may be produced using e-assessment. This may take the form of e-testing (for knowledge and understanding) and/or e-portfolios (for practical abilities). There is no requirement for you to seek prior approval if you wish to use e-assessment for either of these purposes so long as the normal standards for validity and reliability are observed. Please see the following SQA publications for further information on e-assessment: (1) "SQA Guidelines on Online Assessment for Further Education" (March 2003) and (2) "Assessment & Quality Assurance in Open & Distance Learning" (Feb. 2001).

If a centre is presenting Outcome 1 of these assessments on-line the following assessment methods, where appropriate, may be selected –

- Multiple-choice
- Drag and drop
- Multiple response
- Mix and match
- A combination of the above

It is expected that the questions will be of the multi-choice variety. Centres may consider the use of alternative questions types, particularly if using Computer Assisted Assessment approaches. However, care should be taken that the questions are valid and at an appropriate level. The use of simple true/false question responses is unlikely to achieve this.

Since the core skill of Numeracy at Intermediate 2 is embedded in this Unit, it is strongly recommended that you follow the assessment guidelines given. If you wish to use a different assessment model you should seek prior moderation of the assessment instrument(s) you intend to use to ensure that the core skill is still covered. Please note, candidates must achieve all of the minimum evidence specified for each Outcome, combination of Outcomes, or for the Unit as a whole in order to pass the Unit and achieve the core skill.

Higher National Unit specification: statement of standards

Unit title: Computer Architecture 1

Unit Code: DH2T 34

The sections of the Unit stating the Outcomes, knowledge and/or skill, and evidence requirements are mandatory.

Where evidence for an Outcome is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Demonstrate an ability to manipulate and translate data representations.

Knowledge and/or skills

- How to convert between different number bases using integer numbers, eg denary to hexadecimal, hexadecimal to denary, denary to binary, binary to denary, binary to hexadecimal and hexadecimal to binary
- How to perform arithmetic operations in different number bases
- How to carry out Boolean logic operations
- How American Standard Code for Information Interchange (ASCII) characters are represented in computer storage
- How characters are represented using modern character encoding standard

Evidence requirements

Evidence for all the knowledge and/or skills in this Outcome will be assessed using 20 multiple-choice questions. The questions presented must change on **each** assessment occasion. All Evidence Requirements must be covered at least ONCE with additional questions at the discretion of the centre.

1. Perform addition and subtraction between two binary values and two hexadecimal values not less than one byte long
2. Convert
   - integer numbers in base ten (denary) to base sixteen (hexadecimal) and base sixteen to base ten
   - integer numbers in base ten (denary) to base two (binary) and base two to base ten
   - integer numbers in base two (binary) to base sixteen (hexadecimal)
   - integer number in base sixteen (hexadecimal) to base two
3. Apply standard Boolean operators (AND, OR, XOR and NOT) in relation to gates with binary inputs not less than eight bits.
4. Convert 7-bit ASCII text to binary, and binary values to 7-bit ASCII.
5. Convert modern character representations to characters and characters to modern character representations.

Higher National Unit specification: statement of standards (cont)

Unit title: Computer Architecture 1

If a centre is presenting this assessment on-line the following assessment methods, where appropriate, may be selected –

- Multiple-choice
- Drag and drop
- Multiple response
- Mix and match
- A combination of the above

Assessment guidelines

Assessment must be undertaken in supervised conditions and is closed book. A candidate should complete this assessment within one hour. Candidates may not bring to the assessment event any notes, textbooks, handouts or other material (calculators are not allowed).

Candidates must answer at least 60% of the questions correctly.

There is an opportunity for a candidate to be assessed on-line subject to meeting the prescribed assessment conditions.

Outcome 2

Demonstrate an understanding of the functions of computer system components

Knowledge and/or skills

- Functional components of a computer system
- Physical and functional characteristics of memory
- Communicating with peripheral devices
- Read/write operations
- Interpret graphical/tabular information

Evidence requirements

Each candidate will be required to provide evidence of his/her knowledge and skills for the following:

- Draw a block diagram of the major components of a computer system and bus connections describing the function of each block including the bus functions.

Higher National Unit specification: statement of standards (cont)

Unit title: Computer Architecture 1

- Describe the fundamental types of memory (RAM and ROM) that can be connected to a CPU and the reasons why they are included in a system. The candidate must provide a correct expansion of the name or acronym of at least five different types of memory. The list must be a sample of seven currently available types and must include (i) RAM, (ii) ROM, and could include (iii) DRAM, (iv) PROM, (v) SRAM, (vi) EPROM, (vii) Flash memory. Describe the terms access speed and cycle time.
- Differentiate between polling and interrupts as a way of transferring data between the CPU and peripheral devices. The candidate must correctly state, for two scenarios, whether a scenario describes a polled or interrupt driven approach. Any major disadvantages of the
- approach should be correctly stated. The scenarios need not be confined to computer systems, as long as the distinction between the two approaches remains clear.
- Detail the sequence of events when a system performs activities using the system bus. The candidate must correctly trace the sequence of activities on the system buses for at least two different activities, sampled from (i) reading from memory, (ii) writing to memory, (iii) writing to an I/O port, (iv) reading from an I/O port. Such traces must not contain error rates higher than one error per eight steps.
- Interpret graphical/tabular information from supplied materials.

Assessment for this Outcome must be based on ALL of the five items above. Different assessment events must sample different subsets. Alternative assessment instruments must use different values/scenarios as far as possible.

Assessment guidelines

Assessment is open book under supervised conditions and reference will be permitted to textbooks, handouts or other material that candidates have prepared for themselves. Assessors should assure themselves of the authenticity of each candidate's submission.

Minor errors are acceptable but must be kept to a minimum (excluding the fifth bullet point in the Knowledge and Skills where a candidate must answer accurately); **two** errors in total are allowed covering the remaining outcome knowledge and skills bullet points. The achievement requirements are inherent in the evidence requirements.

Higher National Unit specification: statement of standards (cont)

Unit title: Computer Architecture 1

Outcome 3

Demonstrate an understanding of the principles of Central Processor Unit (CPU) operation

Knowledge and/or skills

- Internal elements of the CPU
- Fetch/execute cycle which will include how machine operations are organised and represented

Evidence requirements

The candidate should provide evidence to demonstrate his/her ability to:

- State the function and operation of all the internal components of the processor including timing and control unit, decoder, instruction register, data buffer, MAR (memory address register), PC (program counter), general purpose register and ALU (arithmetic and logic unit).
- Detail the activities involved in the fetch/execute cycle. The candidate will be required to provide a trace of the activities of the processor as it performs two different assembly level instructions. One instruction should be adding a value from memory to the accumulator; the second should be an indirect load of a value from memory to a general-purpose register. Evidence will be collected on a supplied pro-forma with spaces to record the values in registers as they change when the cycles of the fetch/execute cycle progress. The candidate must complete this exercise with no higher an error rate than one step in ten.

Assessment for this Outcome must be based on all of the topics detailed above. Alternative assessment instruments must use different values/scenarios.

Assessment guidelines

Assessment is open book under supervised conditions and reference will be permitted to textbooks, handouts or other material that candidates have prepared for themselves. Assessors should assure themselves of the authenticity of each candidate's submission.

Minor errors are acceptable but must be kept to a minimum; two errors in total are allowed covering ALL the outcome knowledge and skills bullet points. The achievement requirements are inherent in the evidence requirements.

Administrative information

Unit Code: DH2T 34

Unit Title: Computer Architecture 1

Superclass category: CA

Date of Publication: June 2004

Source: SQA

Higher National Unit specification: support notes

Unit title: Computer Architecture 1

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the Centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

This Unit is primarily intended to provide an insight into the mechanisms that underlie the operation of digital computers. The concepts and principles are likely to impact the computer professional on a day-to-day basis.

Software developers are likely to need to understand the implications of number systems so that informed decisions can be made about the choice of variable types when programming.

Support staff will be faced with the need to perform base conversions when installing hardware.

Guidance on Delivery and Assessment

Outcome 1

Delivery

This Outcome concentrates on the representational issues within computing, working on the basic premise that computer professionals should have a grounding in how data is represented, and the procedure by which values are converted between the computer representation and representations that humans are more familiar with.

As it can be safely assumed that any of these representational issues will form part of the day-to-day activities of those working in the computing industry, a broad range of topics can be presented with the intention of raising candidate's awareness of the broad range of the subject.

As far as possible the topics should be delivered in such a way that the practical uses and implications of the subject are made clear to candidates.

Some grounding in number systems (especially those using positional representation) will benefit candidates. It may be useful to introduce other numbering systems, such as Roman, so that the benefits of different types of system can be discussed. If needed, candidates could be reminded of techniques required to complete this topic. Techniques required will include long division and multiplication. It may be advantageous to both tutor and candidate to discuss the use of number bases in everyday life, for example, base 60, (hours/minutes/seconds), base 7, (days/weeks), base 24, (hours/days). The realisation that candidates are already capable of working in different bases may help to reduce the amount of trepidation some may have regarding this subject area.

In particular candidates should be introduced to:

1. Use of Boolean operators. Although of particular interest to those intending to pursue the subject of computer networks as a specialism, this topic will also be of benefit to those who wish to work with low level programming, eg in the increasingly important area of micro-controllers. Although not assessed, Centres may also wish to introduce other operators, such as NAND.
2. Understanding the relationship between the number of bits in a binary value and the range of values that can be held in that number of bits is of use in software development where the choice of the correct type of variable can be informed by this knowledge. Centres may wish to highlight the relationship between size of representation and speed.
3. The study of the representation of ASCII characters as binary patterns can be used to highlight the idea that all data held by a computer system is held in a binary representation, and this can be reinforced by the use of representing colours (and perhaps other analogue quantities) in a digital format.
4. Performing addition and subtraction at the binary level can be used to illustrate the level at which the machine works and reinforce the representational issues.

Some Centres may wish to supplement traditional teaching methods with software packages that allow candidates extra practice.

As the material covered in this topic underpins much of the rest of the material in the Unit, and indeed computing in general, it is suggested that it is delivered early in the Unit and early in the group award. As the Unit unfolds, opportunities can be taken to reinforce the material and place it in context.

Assessment

This is largely a practical topic and it seems sensible to assess on the basis of candidates' demonstrating practical abilities. A Centre will find that this assessment can be carried out as one supervised session.

The skills gained in this section require that candidates display the ability to manipulate the representations used within the computer, and the majority of these are numerical. Assessments should reflect the numerate nature of this section of the Unit.

The ease with which numerical questions can be set should not be taken as an excuse by Centres to over assess this topic, as this may be at the expense of teaching time. Given the nature of the topic it is suggested that the material should not be assessed by questions requiring narrative answers.

Given that some assessment may relate to other Units, such as installing hardware, calculating network masks or calculating image file size, opportunities could be investigated to integrate suitable assessments.

Whilst advice is given to deliver the material early in the course, Centres may find that assessment is best delayed until candidates have had the opportunity to gain sufficient practice in using the procedures.

Higher National Unit specification: support notes (cont)

Unit title: Computer Architecture 1

Outcome 2

Delivery

As this topic is largely based in hardware, it is suggested that candidates are actually shown some hardware as part of the course. Such devices as memory should be readily available to centres. Of particular benefit are EPROMS with a quartz window through which the silicon is visible. This can be used to both suggest the physical reality of the devices and the regular structure of the device. The internal components of a CPU, such as the ALU and Instruction decoder could be presented as parts of an interdependent community, with each unit having a specific purpose. Additional to the traditional teaching methods, a role-play exercise could be carried out, with participants playing the role of different components, or a software animation could be used. These methods could also be used to enhance the learning experience.

The idea of different vendors having slightly different architectures could be introduced in this section, but with emphasis being made on the taught model. As new memory devices reach the market they should be considered for inclusion in this section. The role of cache RAM in improving system performance should be explained.

The exposition of the issues between polling and interrupts can be augmented with either a software simulation or a series of role-play exercises. Priority and the details of interrupt handling can be discussed here, with the caveat that different models are possible.

Assessment

The skills learned for this Outcome relate to the practical activities or characteristics of hardware devices. Assessment should reflect the practical nature of the course and concentrate on ensuring that candidates do actually know what is happening 'under the hood'. This is probably best done by using numerical or graphical descriptions of processes.

To ensure authenticity, this Outcome must be assessed as in-class open book assessment in supervised conditions. Where time permits this could be performed in a single session, some Centres may prefer to run two shorter sessions.

The ease with which numerical questions can be set should not be taken as an excuse by centres to over assess this topic, as this may be at the expense of teaching time.

Given the nature of the topic it is suggested that the material should not be assessed by questions requiring narrative answers.

This assessment also covers part of the Numeracy core skill (ie bullet point 5) and must be answered by a candidate correctly.

Higher National Unit specification: support notes (cont)

Unit title: Computer Architecture 1

Outcome 3

This Outcome focuses on the activities within the system, and as such, much of the teaching could be performed as traces of activity, role-play or with software simulations.

The first section concerns the fetch/execute cycle. It would probably be best to introduce this with an exposition of the components of the CPU (revised from Outcome 2) and an overview of some simple assembly level instructions. Whilst the candidate is not required to write any assembly level programs for this Unit, an understanding of the processes will be of benefit, especially for the execute part of the cycle. The internal registers of the CPU, such as MAR, and MDR should also be introduced and explained.

An example trace of a few instructions will probably prove instructive.

Assessment

The assessment for this Outcome is intended to take advantage of the way that much of the evidence can be collected numerically or graphically. This Outcome should be assessed by open book methods, which most Centres will find most convenient to do as an in-class event in supervised conditions. Centres may decide to perform this either as three single topic assessments, which will increase the administrative load or as a single larger assessment that will increase the cognitive load on candidates. The ease with which numerical questions can be set should not be taken as an excuse by centres to over assess this topic, as this may be at the expense of teaching time

Open learning

If this Unit is delivered by open or distance learning methods, additional planning and resources may be required for candidate support, assessment and quality assurance. A combination of new and traditional authentication tools may have to be devised for assessment and re-assessment purposes. For further information and advice, please see *Assessment and Quality Assurance for Open and Distance Learning* (SQA, February 2001 — publication code A1030).

Special needs

This Unit specification is intended to ensure that there are no artificial barriers to learning or assessment. Special needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments or considering special alternative Outcomes for Units. For information on these, please refer to the SQA document *Guidance on Special Assessment Arrangements* (SQA, 2001).

General information for candidates

Unit title: Computer Architecture 1

This Unit is designed to introduce you to, and enable you to understand the concepts of Computer Architecture. On completion of the Unit you should be able to:

1. Demonstrate an ability to manipulate and translate data representations
2. Demonstrate an understanding of the functions of computer system components
3. Demonstrate an understanding of the principles of Central Processor Unit Operation.

In Outcome 1 you will learn how to represent and manipulate data in a computer system. Computer professionals should have a good grounding in how data is represented, and the procedure by which values are converted between the computer representation and representations that humans are more familiar with. This will involve you in learning about number bases, eg: denary, binary, hexadecimal, and how to convert numbers between number bases. You will also learn about Boolean logic operations, truth tables and text representations.

In Outcome 2 you will learn about processors, memory, input/output, buses, polling and interrupts. You will also see the sequence of events when a processor accesses memory and I/O devices.

In Outcome 3 you will learn about how machine operations are organised and represented; the different addressing modes used by the processor and the fetch/execute cycle.

Assessment will be mainly through questions that aim to test your knowledge of the areas of Computer Architecture set out above. There is a closed book assessment only for Outcome 1. Outcomes 2 and 3 are open book and reference will be permitted to textbooks, handouts or other material that you have prepared yourself.