-SQA-SCOTTISH QUALIFICATIONS AUTHORITY

HIGHER NATIONAL UNIT SPECIFICATION

GENERAL INFORMATION

-Unit Number- **2451847**

-Superclass- **XL**

-Title- **MICROPROCESSOR SYSTEM FUNDAMENTALS**

-DESCRIPTION-

GENERAL COMPETENCE FOR UNIT: Use a microprocessor system and using applications programmes.

OUTCOMES

1. analyse the operation of a microprocessor based system;
2. use programmable parallel interface devices;
3. analyse I/O data transfer techniques;
4. apply serial data transfer techniques.

CREDIT VALUE: 1 HN Credit

ACCESS STATEMENT: Access to this unit is at the discretion of the centre. However, it may be beneficial if the candidate had prior knowledge of assembly language programming. This may be evidenced by possession of NC module:

3150624 Program Controlled Systems

or similar qualifications or experience.

For further information contact: Committee and Administration Unit, SQA, Hanover House, 24 Douglas Street, Glasgow G2 7NQ.

Additional copies of this unit may be purchased from SQA (Sales and Despatch section). At the time of publication, the cost is £1.50 (minimum order £5.00).

HIGHER NATIONAL UNIT SPECIFICATION

STATEMENT OF STANDARDS

UNIT NUMBER: 2451847

UNIT TITLE: MICROPROCESSOR SYSTEM FUNDAMENTALS

Acceptable performance in this unit will be the satisfactory achievement of the standards set out in this part of the specification. All sections of the statement of standards are mandatory and cannot be altered without reference to SQA.

OUTCOME

1. ANALYSE THE OPERATION OF A MICROPROCESSOR BASED SYSTEM

PERFORMANCE CRITERIA

(a) The description of the main functional blocks of a microprocessor based system is correct.
(b) The technique of address decoding is correctly described in relation to the allocation of address ranges for memory and input/output devices.
(c) The explanation of the basic instruction cycle is correct.
(d) The advantages and disadvantages of a microprocessor based system over a hard wired logic system are correctly described with reference to speed, cost, functionality and versatility.

RANGE STATEMENT

Functional blocks: memory; CPU; programmable input/output devices; system busses; clock.

Address range: 16 address lines; 16 x 4k chips; high order and low order addresses; Chip select.

Instruction cycle: system busses; fetch and execute cycles.

EVIDENCE REQUIREMENTS

Written and graphical evidence of the candidate's ability to analyse the operation of a microprocessor based system, as stated in performance criteria (a) to (d).

OUTCOME

2. USE PROGRAMMABLE PARALLEL INTERFACE DEVICES

PERFORMANCE CRITERIA

(a) Parallel and serial data transfer techniques are critically compared with reference to speed, cost, distance and application.
(b) The use of a parallel interface is correct with reference to basic input/output.
(c) The use of a counter/timer device is correct.
(d) The description of hardware and software methods for prioritising interrupt devices is correct.

RANGE STATEMENT

The range for this outcome is fully expressed in the performance criteria.

EVIDENCE REQUIREMENTS

Written evidence of the candidate's ability to compare data transfer techniques detailed in performance criteria (a).

Performance evidence of the candidate's ability to use the devices as detailed in performance criteria (b) and (c).

OUTCOME

3. ANALYSE I/O DATA TRANSFER TECHNIQUES

PERFORMANCE CRITERIA

(a) The explanation of handshaking signals used to synchronise data transfer is correct.
(b) The explanation of interrupt driven I/O is correct.
(c) The description of hardware and software methods for prioritising interrupt devices is correct.

RANGE STATEMENT

Methods of prioritising interrupts: priority interrupt controller; polling.

EVIDENCE REQUIREMENTS

Written evidence of the candidate's ability to describe the devices in performance criteria (a) (c).

OUTCOME

4. APPLY SERIAL DATA TRANSFER TECHNIQUES

PERFORMANCE CRITERIA

(a) The description of the features of an a synchronous serial interface is correct with reference to framing parity and clock rate.
(b) The use of a software routine to configure a serial interface and transmit and receive characters is correct.
(c) Common serial interface standards are compared with reference to speed, distance, voltage level and application.

RANGE STATEMENT

Serial interface standards: RS232, RS485, RS422, RS423.

EVIDENCE REQUIREMENTS

Written and graphical evidence of the candidate's ability to describe and compare the techniques as detailed in performance criteria (a) and (c).

Performance evidence of the candidate's ability to use software as detailed in performance criterion (b).

MERIT To gain a pass in this unit, a candidate must meet the standards set out in the outcomes, performance criteria, range statements and evidence requirements.

To achieve a merit in this unit, a candidate must demonstrate a superior or more sophisticated level of performance. This may be demonstrated by:

(i) analytical skills;
(ii) logical presentation of work.

ASSESSMENT

In order to achieve this unit, candidates are required to present sufficient evidence that they have met all the performance criteria for each outcome within the range specified. Details of these requirements are given for each outcome. The assessment instruments used should follow the general guidance offered by the SQA assessment model and an integrative approach to assessment is encouraged. (See references at the end of support notes).

Accurate records should be made of the assessment instruments used showing how evidence is generated for each outcome and giving marking schemes and/or checklists, etc. Records of candidates' achievements should be kept. These records will be available for external verification.

SPECIAL NEEDS

Proposals to modify outcomes, range statements or agreed assessment arrangements should be discussed in the first place with the external verifier.

HIGHER NATIONAL UNIT SPECIFICATION

SUPPORT NOTES

UNIT NUMBER: 2451847

UNIT TITLE: MICROPROCESSOR SYSTEM FUNDAMENTALS

SUPPORT NOTES: This part of the unit specification is offered as guidance. None of the sections of the support notes is mandatory.

NOTIONAL DESIGN LENGTH: SQA allocates a notional design length to a unit on the basis of time estimated for achievement of the stated standards by a candidate whose starting point is as described in the access statement. The notional design length for this unit is 40 hours. The use of notional design length for programme design and timetabling is advisory only.

PURPOSE The purpose of this unit is to develop an understanding of the principles of microprocessor systems.

CONTENT/CONTEXT

Outcome 1

Using a block diagram describe the standard 8 bit computer system. Explain that the principles apply to modern 32 bit machines. Discuss bus structures and the use of timing to determine which signals are present on the bus.

Describe simple decoding techniques and how bus contention is prevented by enabling only one device at a time. Explain that high order addresses are used to select a device.

Describe the steps involved in the fetch/execute cycle. Use simplified read/write waveforms to illustrate the cycle.

Outcome 2

State the data transfer methods employed with the common peripheral devices eg. mouse, keyboard, printer, modem etc.

Interface devices could include PPI8255 and CTC8253.

Discuss the features and applications of the devices.

Typical application of the 8253 is closed loop control of a DC motor using pulse width modulation.

Outcome 3

Examples of handshaking signals could include a printer interface (Strobe and Busy signals) and A/D converter interface (End of convert and Start of convert signals).

Outcome 4

UART: features to include start bit, data length, parity bit, stop bits and data rate.

Software used to transmit and receive data from a protocol analyser or a dedicated circuit.

ASSESSMENT PROCEDURES Centres may use Instruments of Assessment which are considered by tutors to be most appropriate.

Outcomes 1, 2, and 3 could be assessed using 10-20 short answer or restricted response questions, or suitable oral questions, balanced appropriately across the performance criteria.

Outcome 4 could be assessed using a checklist covering the main practical activities of performance criteria (a) to (d).

PROGRESSION Achievement of this unit would provide a sound basis for access to the more specialised HN unit 2451837 Microprocessor Systems Design.

REFERENCES

1. Guide to unit writing.
2. For a fuller discussion on assessment issues, please refer to SQA's Guide to Assessment.
3. Information for centres on SQA's operating procedures is contained in SQA's Guide to Procedures.
4. For details of other SQA publications, please consult SQA's publications list.