National Unit Specification: general information

UNIT Combinational Logic (SCQF level 6)

CODE F5H9 12

SUMMARY

This Unit develops the candidate's knowledge of the devices, circuits and techniques of digital electronics from basic gates to Medium Scale Integrated (MSI) devices. Candidates will investigate the logical characteristics of arithmetic circuits and data conversion circuits first using basic gates and extend the applications of digital electronics devices and techniques to using MSI devices. This Unit is suitable for candidates wishing to progress a career in electronic engineering. It is also suitable for candidates studying other branches of engineering, science, computing or technology.

This Unit may form part of a National Qualification Group Award or may be offered on a free standing basis.

OUTCOMES

1 Construct Arithmetic Circuits and investigate their function.
2 Investigate Combinational Data Conversion Circuits.
3 Investigate and test MSI Logic Devices.

RECOMMENDED ENTRY

While entry is at the discretion of the centre, candidates would normally be expected to have attained one of the following, or equivalent:

- Standard Grade in a Science or Technology subject — General Level
- NQ Unit *Combinational Logic* (SCQF level 5)

Administrative Information

Superclass: XL

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National Unit Specification: general information (cont)

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CREDIT VALUE

1 credit at SCQF level 6 (6 SCQF credit points at SCQF level 6*).

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

CORE SKILLS

There is no automatic certification of Core Skills in this Unit.

This Unit provides opportunities for candidates to develop aspects of the following Core Skills:

- Numeracy (SCQF level 6)
- Problem Solving (SCQF level 6)
- Communication (SCQF level 6)

These opportunities are highlighted in the Support Notes of this Unit Specification.

National Unit Specification: statement of standards

UNIT Combinational Logic (SCQF level 6)

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the Unit Specification. All sections of the statement of standards are mandatory and cannot be altered without reference to SQA.

OUTCOME 1

Construct Arithmetic Circuits and investigate their function.

Performance Criteria

(a) Correctly construct and investigate a 3 input FA adder cell using 2 HA cells and an OR gate.
(b) Correctly investigate the 2's Complement Number System.
(c) Correctly construct 4-bit adder/subtractor using 4-bit parallel adder module and XOR gates.

OUTCOME 2

Investigate Combinational Data Conversion Circuits.

Performance Criteria

(a) Correctly investigate 2 to 4 line Decoders and 4 to 2 line Encoders.
(b) Correctly investigate 4 to 1 line multiplexer (MUX) and 1 to 4 line demultiplexer (DEMUX).

OUTCOME 3

Investigate and test MSI Logic Devices.

Performance Criteria

(a) Correctly investigate and test MSI Arithmetic devices.
(b) Correctly investigate and test MSI Encoder/Decoder devices.
(c) Correctly investigate and test MSI Multiplexer/Demultiplexer devices.

National Unit Specification: statement of standards (cont)

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EVIDENCE REQUIREMENTS FOR THIS UNIT

Evidence is required to demonstrate that candidates have achieved all Outcomes and Performance Criteria.

Performance evidence as well as written and/or recorded oral evidence is required which demonstrates that the candidate has achieved all Outcomes to the standards specified in the Outcome and Performance Criteria. A record of successfully completed test specifications for each circuit and device, as specified in the Performance Criteria, must be included and retained by the centre.

This evidence should be produced under supervised, controlled conditions at appropriate points throughout the Unit either on an Outcome by Outcome basis or as integrated assessments. All calculations and measurements should be given using the relevant SI units of measurement.

The required evidence for all Outcomes, is as follows:

For Outcome 1:

- correctly Pin assigned circuit diagram for FA
- correct layout diagram for FA
- FA Circuit construction is correct
- FA Circuit test specification results are correct
- FA Circuit description of capability is correct
- FA Circuit description of operation is correct
- addition and subtraction is performed correctly for two 4-bit words including sign bit
- 4-bit adder/subtractor construction is correct
- 4-bit adder/subtractor test specification results are correct
- 4-bit adder/subtractor description of capability is correct
- 4-bit adder/subtractor description of operation is correct

For Outcome 2:

- correctly Pin assigned circuit diagram for each Data Conversion circuit
- correct layout diagram for each Data Conversion circuit
- Data Conversion Circuits are constructed correctly
- Data Conversion Circuit test specification results are correct
- Data Conversion Circuit descriptions of capability are correct
- Data Conversion Circuit description of operation is correct

For Outcome 3:

- Pin assigned circuit diagrams for each device are correct
- Construction Layout Diagrams for each device are correct
- MSI Device construction for each device is correct
- MSI Device test specification results for each device are correct
- MSI Device description of capability for each device is correct
- MSI Device description of operation for each device is correct

National Unit Specification: statement of standards (cont)

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The Assessment Support Pack for this Unit provides sample assessment material. Centres wishing to develop their own assessments should refer to the Assessment Support Pack to ensure a comparable standard.

National Unit Specification: support notes

UNIT Combinational Logic (SCQF level 6)

This part of the Unit Specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

GUIDANCE ON THE CONTENT AND CONTEXT FOR THIS UNIT

This is a restricted core Unit within the National Certificate in Electronic Engineering at SCQF level 6. It may also form part of other National Qualification Group Awards in Engineering and can also be taken as a free-standing Unit.

The circuits constructed and investigated in Outcome 1 and Outcome 2 may be constructed and tested using breadboard or other practical prototyping methods.

The principles and methods developed in Outcomes 1 and 2 can be extended and applied using suitable TTL or CMOS MSI devices.

GUIDANCE ON LEARNING AND TEACHING APPROACHES FOR THIS UNIT

The approach to learning and teaching in this Unit is through practical investigation, discussion and demonstration. A workbook should be kept where the candidate records the results of their investigations and conclusions, hence indicating their progress and providing a record of activities carried out. The workbook should also clearly indicate exercises that are of sufficient merit to count towards a summative assessment candidate folio. The workbook should also demonstrate the full range of work carried out, both good and bad, that has contributed to the candidates understanding.

The workbook could contain device pin-out diagrams, pin assigned circuit diagrams, construction layout diagrams, extracts from relevant datasheets etc. All relevant construction details and test methods used for each device and circuits investigated could be included along with candidate's descriptions of device/circuit operations.

The emphasis in Outcomes 1 and 2 is developing an understanding of how basic gates can be used to realise Arithmetic Circuits, Encoding/Decoding Circuits and Multiplexing/Demultiplexing circuits.

The background theory such as Binary Addition, Addition and Subtraction using the 2's Complement system should be explored and examples worked through before realising the associated logic circuitry. The learning should be developed progressively, concept, basic gates, circuit/module, to the MSI Devices of Outcome 3 eg concept of binary addition, the XOR gate and AND gate, Half Adder Circuit, Full Adder Module, 4-bit Parallel Adder MSI device, which can itself be used as a component in a larger system.

Candidates should be encouraged to discuss between themselves how the basic gates relate to the MSI devices and have time to build and investigate the operation of the basic gate modules before going on to investigate how to use/drive the MSI devices leading to a better understanding of how the MSI devices operate.

National Unit Specification: support notes (cont)

UNIT Combinational Logic (SCQF level 6)

OPPORTUNITIES FOR CORE SKILL DEVELOPMENT

The ability to interpret, translate, convert and apply complex numerical and graphic data is integral to achievement. *Numeracy* skills will be naturally enhanced with a focus on the practical interpretation, use and presentation of number and graphics.

Elements of the Core Skill of *Problem Solving*, that is, Critical Thinking, Planning, and Organising, can be developed as candidates undertake construction, investigations and testing. Evaluation of relevant technical information would provide underpinning knowledge and strengthen analytical reading skills. All relevant construction details, test methods and results are recorded in the workbook. Candidates should be advised on acceptable formats, terminology and structures for written evidence. Group investigation, discussion and demonstration would support reflective review of achievement and enhance skills in Oral Communication element of the Core Skill *Communication*.

GUIDANCE ON APPROACHES TO ASSESSMENT FOR THIS UNIT

Opportunities for the use of e-assessment

E-assessment may be appropriate for some assessments in this Unit. By e-assessment we mean assessment which is supported by information and communications technology (ICT), such as e-testing or the use of e-portfolios or e-checklists. Centres which wish to use e-assessment must ensure that the national standard is applied to all candidate evidence and that conditions of assessment as specified in the Evidence Requirements are met, regardless of the mode of gathering evidence. Further advice is available in *SQA Guidelines on Online Assessment for Further Education (AA1641, March 2003), SQA Guidelines on e-assessment for Schools (BD2625, June 2005).*

The required evidence can be generated throughout by means of Practical Investigation/Assignments covering all three Outcomes developed over the course of the Unit. The activities carried out during the practical investigation/assignments being recorded in a workbook. A candidate folio of work covering the Outcomes and Performance Criteria, selected from the workbook, should be submitted near the end of the Unit with sufficient time for feedback and remediation

For all Outcomes the test circuits may be constructed using breadboard, pluggable logic tutor, prototyping board such as stripboard or similar, the more complex 4-bit adder subtractor circuit could be constructed on pre-printed PCB. Construction exercises could be combined as an exercise with the Units *Practical Electronics* and *Soldering and Circuit Assembly Techniques*.

DISABLED CANDIDATES AND/OR THOSE WITH ADDITIONAL SUPPORT NEEDS

The additional support needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments, or considering whether any reasonable adjustments may be required. Further advice can be found on our website **www.sqa.org.uk/assessmentarrangements**