National Unit Specification: general information

UNIT Sequential Logic (SCQF level 5)

CODE F5JR 11

SUMMARY

The Unit explores the devices, circuits and techniques of sequential logic. Candidates will investigate the operation of latches and bistables. Applications such as Counter and Register circuits are developed. The resulting circuits are then built and tested. This Unit is suitable for candidates wishing to embark upon a career in electronic engineering. It is also suitable for candidates studying other branches of engineering, science, computing or technology.

This Unit may form part of a National Qualification Group Award or may be delivered on a free-standing basis.

OUTCOMES

1 Investigate Sequential Logic characteristics of Cross-coupled gates.
2 Investigate the operation of Clocked bistables.
3 Investigate the operation of Counter and Register Circuits.

RECOMMENDED ENTRY

While entry is at the discretion of the centre, candidates would normally be expected to have attained one of the following, or equivalent:

- Standard Grade in a Science or Technology subject — General Level

Administrative Information

Superclass: XL

Publication date: March 2009

Source: Scottish Qualifications Authority

Version: 01

National Unit Specification: general information (cont)

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CREDIT VALUE

1 credit at SCQF level 5 (6 SCQF credit points at SCQF level 5*).

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

CORE SKILLS

There is no automatic certification of Core Skills in this Unit.

This Unit provides opportunities for candidates to develop aspects of the following Core Skills:

- Communication (SCQF level 5)

These opportunities are highlighted in the Support Notes of this Unit Specification.

National Unit Specification: statement of standards

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Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the Unit Specification. All sections of the statement of standards are mandatory and cannot be altered without reference to SQA.

OUTCOME 1

Investigate Sequential Logic characteristics of Cross-coupled gates.

Performance Criteria

(a) Verify correctly the operation of Cross-coupled NAND or NOR gates.
(b) Correctly identify the modes of operation of the SR latch.
(c) Verify correctly the actions of the SR latch with waveform timing diagrams.

OUTCOME 2

Investigate the operation of Clocked bistables.

Performance Criteria

(a) Verify correctly modes of operation for bistables.
(b) Verify correctly level and edge sensitivity of clocked bistables.
(c) Investigate correctly actions of bistables from given waveform timing diagrams.

OUTCOME 3

Investigate the operation of Counter and Register Circuits.

Performance Criteria

(a) Verify correctly counter circuits using bistables.
(b) Verify correctly shift registers using bistables.
(c) Investigate correctly the actions of counter and register circuits using waveform timing diagrams.

National Unit Specification: statement of standards (cont)

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EVIDENCE REQUIREMENTS FOR THIS UNIT

Evidence is required to demonstrate that candidates have achieved all Outcomes and Performance Criteria.

Performance evidence supplemented with an assessor observation checklist as well as written and/or recorded oral evidence is required which demonstrates that the candidate has achieved all Outcomes to the standards specified in the Outcome and Performance Criteria.

This evidence must be produced under supervised, controlled conditions at appropriate points throughout the Unit either on an Outcome by Outcome basis or as integrated assessments. All calculations and measurements should be given using the relevant SI units of measurement.

The required evidence, for all Outcomes is as follows:

For Outcome 1:

- correctly assembled cross-coupled gate circuit
- accurate record of test results for cross-coupled gate circuit
- clear statement that cross-coupled gates have memory
- clear statement that feedback connections provide memory facility of x-coupled gates
- correct demonstration of operation of latch in terms of S-R inputs and their effect on the latch outputs
- bistable modes of operation are clearly identified on an action table ie Set, Reset, Memory

For Outcome 2:

- correctly assembled bistable test circuits
- modes of operation are clearly identified and accurately recorded on a device action table. ie Set, Reset, Toggle, Memory, Data Transfer, Asynchronous Preset and Clear.
- correct brief statement of bistable operation in terms of synchronous and asynchronous inputs and their effect on outputs
- correctly relates phases of the system clock to bistable sensitivity ie Level Sensitive – High Level or Low Level and Edge sensitive — rising or falling edge

For Outcome 3:

- correctly constructed 4-bit counter circuit using bistables
- correct record of counter operation
- correctly constructed 4-bit register circuit using bistables
- correct record of register operation

National Unit Specification: support notes

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This part of the Unit Specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

GUIDANCE ON THE CONTENT AND CONTEXT FOR THIS UNIT

This is an optional Unit within the National Certificate in Electronic Engineering at SCQF level 5 and can also be delivered as a free-standing Unit.

The importance of memory should be outlined throughout with examples of modern day systems that rely on memory for their operation. It should be made clear that the gates used to construct combinational logic circuits do not have memory but devices such as bistables and latches constructed from basic gates can have memory. Examples can be used where information is stored or event occurrences are latched for later use.

Candidates should cover sufficient material and be given adequate time to develop the necessary understanding of the content outlined below.

Draw cross-coupled gate circuits, Pin assign circuit diagrams for testing latches and bistables. Draw up Action Tables for each type of latch or bistable. Construct latch and bistable test circuits and accurately record test results on action tables for the cross-coupled latches and bistables. Candidates should also correctly describe the operation of the cross-coupled gates, latches and bistables with reference to synchronous and asynchronous inputs, modes of operation and bistable outputs.

The need for a system clock in a sequential logic circuits should be illustrated with examples. A real clock signal can be observed on an oscilloscope as a demonstration, the resulting trace redrawn and each phase of the clock examined: eg rising/leading edge — rise time, overshoot, ringing, droop, high level phase, falling/trailing edge — fall time, undershoot, ringing etc. these detailed features can then be shown idealised as a square system clock.

Consequently candidates should be able to identify the active phases of a system clock and relate each phase of the clock to the clock mode of a specific bistable. They should also be given sufficient practice at interpreting clock and input waveform timing diagrams and determining the output conditions for each type of bistable.

Examples of full count sequence and reduced sequence count ripple counters should be explored using the bistable, this should be limited to no more than four stages. Waveform timing diagrams can be used to examine the count sequences and also investigate the reset pulse noise introduced by the reset logic associated with reduced modulus ripple counters. Examples of pre-designed synchronous counters can be used to illustrate the reduced noise associated with synchronous counters.
Shift registers can be investigated using the D-type bistable, again limited to four stages. The common occurrence of registers as data processing units based on the D-type mode of operation should be emphasised as well as arithmetic applications.

The investigations should be based on practical assignments and may be conducted in an informal atmosphere but within a formal laboratory/workshop setting while adhering to relevant safety practices. Candidates may be encouraged to experiment with the bistables and encouraged to work independently at their own pace.

National Unit Specification: support notes (cont)

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GUIDANCE ON LEARNING AND TEACHING APPROACHES FOR THIS UNIT

The approach to teaching and learning in this Unit is through practical investigation, discussion and demonstration. A workbook should be kept where the candidate records the results of their investigations and conclusions; hence indicating their progress and providing a record of activities carried out. The workbook should also clearly indicate exercises that are of sufficient merit to count towards summative assessment. The workbook should also demonstrate the full range of work carried out, both good and bad, that has contributed to the candidates understanding.

The workbook could contain device pin-out diagrams, pin assigned circuit diagrams, construction layout diagrams, extracts from relevant datasheets etc. All relevant construction details and test methods used for each device and circuit investigated could be included along with candidate's descriptions of device/circuit operations.

A record of successfully completed test specifications for each circuit and device specified in the Performance Criteria should be included in the workbook.

Candidates should be encouraged to discuss between themselves how the basic gates provide memory to a digital circuit and have time to build and investigate the operation of the cross-coupled logic gates before going on to investigate how to use them as bistables and subsequently connect them together as sequential logic circuits.

OPPORTUNITIES FOR CORE SKILL DEVELOPMENT

The interpretation of information and data from pin-out diagrams and the need to translate test circuit diagram into a working circuit, which is tested against an action table, provide candidates with opportunities to develop both Written and Oral Communication skills throughout the investigation process.

The physical implementation of the test circuits with gates, latches and bistables presents candidates with a series of problems to be solved, this provides the candidate with an opportunity to develop their *Problem Solving* skills.

GUIDANCE ON APPROACHES TO ASSESSMENT FOR THIS UNIT

Opportunities for the use of e-assessment

E-assessment may be appropriate for some assessments in this Unit. By e-assessment we mean assessment which is supported by information and communications technology (ICT), such as e-testing or the use of e-portfolios or e-checklists. Centres which wish to use e-assessment must ensure that the national standard is applied to all candidate evidence and that conditions of assessment as specified in the Evidence Requirements are met, regardless of the mode of gathering evidence. Further advice is available in *SQA Guidelines on Online Assessment for Further Education (AA1641, March 2003), SQA Guidelines on e-assessment for Schools (BD2625, June 2005).*

National Unit Specification: support notes (cont)

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The required evidence can be generated throughout by means of practical investigation/assignments covering all three Outcomes developed over the course of the Unit. The activities carried out during the practical investigation/assignments being recorded in the workbook. A folio of representative work selected from the workbook will be submitted near the end with sufficient time for feedback and remediation.

For all Outcomes the test circuits may be constructed using breadboard, pluggable logic tutor, prototyping board such as stripboard or similar, progress and results being recorded in candidate's workbook, an observational checklist should also be retained as evidence.

DISABLED CANDIDATES AND/OR THOSE WITH ADDITIONAL SUPPORT NEEDS

The additional support needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments, or considering whether any reasonable adjustments may be required. Further advice can be found on our website **www.sqa.org.uk/assessmentarrangements**