National Unit Specification: general information

UNIT Sequential Logic (SCQF level 6)

CODE F5JS 12

SUMMARY

This Unit further explores the devices, circuits and techniques of sequential logic. Candidates will verify by investigation the characteristics and applications of Counter and Register circuits using Medium Scale Integration (MSI) devices. This Unit is suitable for candidates wishing to progress a career in electronic engineering. It is also suitable for candidates studying other branches of engineering, science, computing or technology.

This Unit may form part of a National Qualification Group Award or may be offered on a free standing basis.

OUTCOMES

1 Verify characteristics and applications of MSI counters.
2 Verify characteristics and applications of MSI shift registers.
3 Verify characteristics and applications of cascaded MSI Counters and Registers.

RECOMMENDED ENTRY

While entry is at the discretion of the centre, candidates would normally be expected to have attained one of the following, or equivalent:

- Standard Grade in a Science or Technology subject – General Level
- NQ Unit: *Sequential Logic* (SCQF level 5)

Administrative Information

Superclass: XL

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National Unit Specification: general information (cont)

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CREDIT VALUE

1 credit at SCQF level 6 (6 SCQF credit points at SCQF level 6*).

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

CORE SKILLS

There is no automatic certification of Core Skills in this Unit.

This Unit provides opportunities for candidates to develop aspects of the following Core Skills:

- Numeracy (SCQF level 6)

These opportunities are highlighted in the Support Notes of this Unit Specification.

National Unit Specification: statement of standards

UNIT Sequential Logic (SCQF level 6)

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the Unit Specification. All sections of the statement of standards are mandatory and cannot be altered without reference to SQA.

OUTCOME 1

Verify characteristics and applications of MSI counters.

Performance Criteria

(a) Correctly verify the count modes and applications of MSI Binary Counters.
(b) Correctly verify the count modes and applications of MSI Decade Counters.

OUTCOME 2

Verify characteristics and applications of MSI shift registers.

Performance Criteria

(a) Correctly verify the shift modes and applications of MSI (Serial In Serial Out) SISO and Serial In Parallel Out (SIPO) shift registers.
(b) Correctly verify the shift modes and applications of MSI (Parallel In Serial Out) PISO and Parallel In Parallel Out (PIPO) shift registers.

OUTCOME 3

Verify characteristics and applications of Cascaded MSI Counters and Registers.

Performance Criteria

(a) Correctly verify the count modes and applications of Cascaded MSI Counters.
(b) Correctly verify the shift modes and applications of Cascaded MSI Registers.

National Unit Specification: statement of standards (cont)

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EVIDENCE REQUIREMENTS FOR THIS UNIT

Evidence is required to demonstrate that candidates have achieved all Outcomes and Performance Criteria.

Performance evidence supplemented with an assessor observation checklist as well as written and/or recorded oral evidence is required which demonstrates that the candidate has achieved all Outcomes to the standards specified in the Outcome and Performance Criteria.

This evidence must be produced under supervised, controlled conditions at appropriate points throughout the Unit either on an Outcome by Outcome basis or as integrated assessments. All calculations and measurements should be given using the relevant SI units of measurement.

The required evidence, for all Outcomes is as follows:

Summary Evidence for Outcomes 1

For 1 MSI Binary counter and 1 MSI Decade counter covering each Performance Criteria the following are correct:

- functional diagrams are developed from device pin-out diagrams
- test circuits are drawn using Pin Assigned functional diagrams
- test circuits are constructed
- test results are recorded
- descriptions of operation of MSI Devices

Summary of Evidence for Outcome 2

For 1 MSI serial and 1 MSI parallel shift register covering each Performance Criteria the following are correct:

- functional diagrams are developed from device pin-out diagrams
- test circuits are drawn using Pin Assigned functional diagrams
- test circuits are constructed
- test results are recorded
- descriptions of operation of MSI Devices

Summary of Evidence for Outcome 3

For 1 Cascaded MSI counter and 1 Cascaded MSI shift register covering each Performance Criteria the following are correct:

- test circuits are drawn using Pin Assigned functional diagrams
- test circuits are constructed
- test results are recorded
- descriptions of Cascaded MSI Devices operation

National Unit Specification: support notes

UNIT Sequential Logic (SCQF level 6)

This part of the Unit Specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

GUIDANCE ON THE CONTENT AND CONTEXT FOR THIS UNIT

This Unit sits within the National Certificate Group Award in Electronic Engineering at SCQF level 6 and can also be delivered as a free-standing Unit.

This Unit extends the knowledge of sequential logic devices and circuits met in the Level 5 Sequential Logic Unit it also complements both the Combinational Logic Level 5 and Level 6 Units consequently a knowledge of associated terminology, theory, gates and bistables is assumed. The circuits constructed and investigated in Outcome 1, Outcome 2 and Outcome 3 are built and tested using breadboard or other practical prototyping system, circuits can also be simulated using suitable software packages. The bulk of the investigation should however be carried out using real devices with reference to common applications of which an indication is given below:

Outcome 1 PCs (a) and (b)

Full modulus binary and decade counters can be explored before going on to implement reduced modulus count sequences. Examples of counter applications such as clock frequency dividers, sequence generation, sequence controllers can be investigated. The investigations of binary and decade counters may be achieved using appropriate MSI devices.

Outcome 2 PCs (a) and (b)

Simple SISO, SIPO, PISO and PIPO shift register configurations can be investigate using suitable MSI devices before going on to explore shift register applications such as arithmetic shift, data storage and delay, code generation and sequence detection etc.

Outcome 3 PCs (a) and (b)

The Counter and Register MSI devices investigated in Outcomes 1 and 2 can be cascaded to meet the requirements of Outcome 3 allowing for larger count sequences and longer shift register applications to be explored.

GUIDANCE ON LEARNING AND TEACHING APPROACHES FOR THIS UNIT

The approach to teaching and learning in this Unit is through practical investigation, discussion and demonstration. A workbook should be kept where the candidate records the results of their investigations and conclusions, hence indicating their progress and providing a record of activities carried out.

After an introduction to the advantages of MSI devices over circuits built using discrete gates and bistables the importance of signal naming conventions regarding activity levels can be discussed. This leads into candidate centred, resource based learning where appropriate construction hardware and measurement instruments are available throughout. A mixture of construction mediums can be used such as logic tutors, breadboard and stripboard etc.

In Outcomes 1 and 2 the concepts required to drive MSI counters and shift registers are developed, this could be introduced by working with device data sheets and application notes, candidates become familiar with the signal names used and device configurations possible. Time can be spent considering and discussing the implied function of each, waveform timing diagrams/application notes can also be explored. Resulting from their considerations candidates develop a functional diagram to represent the MSI device. The functional diagram is drawn with input signals on the left and output signals to the right, control inputs can also be placed on the left or at the top or bottom of the functional diagram outline where convenient. The functional diagram is then pin assigned and used as a basis for a test circuit with appropriate inputs and outputs connected. The circuits can then be constructed and driven by the candidate to perform the various operations required of counters and shift registers outlined in the appropriate PC.

For Outcome 3 candidates identify cascading inputs and outputs that can be used to connect together two or more MSI devices in cascaded mode to extend the count range and shift depth of each MSI device.

Candidates should be encouraged throughout to experiment and discuss between themselves the functions of each MSI device and have several opportunities to drive and use the single MSI devices before going on to investigate the cascade modes.

OPPORTUNITIES FOR CORE SKILL DEVELOPMENT

Providing descriptions of circuit operation and device capabilities and being encouraged to discus their results and how the circuits operate provide candidates with opportunities to develop written and oral communication skills.

Translation of information in diagrams, application notes and device data sheets; development of functional diagrams and determination of test specifications will provide opportunities to develop *Numeracy* skills.

GUIDANCE ON APPROACHES TO ASSESSMENT FOR THIS UNIT

Opportunities for the use of e-assessment

E-assessment may be appropriate for some assessments in this Unit. By e-assessment we mean assessment which is supported by information and communications technology (ICT), such as e-testing or the use of e-portfolios or e-checklists. Centres which wish to use e-assessment must ensure that the national standard is applied to all candidate evidence and that conditions of assessment as specified in the Evidence Requirements are met, regardless of the mode of gathering evidence. Further advice is available in *SQA Guidelines on Online Assessment for Further Education (AA1641, March 2003), SQA Guidelines on e-assessment for Schools (BD2625, June 2005).*

National Unit Specification: support notes (cont)

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The required evidence can be generated throughout by means of Practical Investigation/Assignments covering all three Outcomes developed over the course of the Unit. The activities carried out during the practical investigation/assignments being recorded in a candidate workbook. With a folio of representative work selected from the workbook being submitted near the end with sufficient time for feedback and remediation.

Although the Outcomes are discrete the investigation of each MSI device could be achieved in the context of applications comprising a larger system or sub system. The assessment however should clearly demonstrate the candidate's ability to interpret and drive the MSI devices as single devices and as cascaded devices.

DISABLED CANDIDATES AND/OR THOSE WITH ADDITIONAL SUPPORT NEEDS

The additional support needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments, or considering whether any reasonable adjustments may be required. Further advice can be found on our website **www.sqa.org.uk/assessmentarrangements**