National Unit Specification: general information

UNIT   Combinational Logic (SCQF level 5)

CODE   F5HA 11

SUMMARY

The Unit provides an introduction to the devices, circuits and techniques of digital electronics. Candidates investigate the logical and electrical characteristics of logic gates. From given Boolean expressions logic gates are combined to form combinational logic circuits, which are built and tested. The binary number system used by digital circuits, the decimal number system and the hexadecimal number system are investigated along with methods of conversion between them. This Unit is suitable for candidates wishing to embark upon a career in electronic engineering. It is also suitable for candidates studying other branches of engineering, science, computing or technology

This Unit may form part of a National Qualification Group Award or may be offered on a free standing basis.

OUTCOMES

1   Verify the functions and characteristics of logic gates.
2   Investigate a combinational logic circuit.
3   Investigate a combinational logic circuits to perform numerical operations.

RECOMMENDED ENTRY

While entry is at the discretion of the centre, candidates would normally be expected to have attained one of the following, or equivalent:

♦   Standard Grade in a Science or Technology subject — General Level

Additional copies of this Unit Specification can be purchased from the Scottish Qualifications Authority. Please contact the Customer Contact Centre, telephone 0845 279 1000.

National Unit Specification: general information (cont)

UNIT   Combinational Logic (SCQF level 5)

CREDIT VALUE

1 credit at SCQF level 5 (6 SCQF credit points at SCQF level 5*).

*SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.

CORE SKILLS

There is no automatic certification of Core Skills in this Unit.

This Unit provides opportunities for candidates to develop aspects of the following Core Skills:

♦   Numeracy (SCQF level 5)
♦   Problem Solving (SCQF level 5)

These opportunities are highlighted in the Support Notes of this Unit Specification.

National Unit Specification: statement of standards

UNIT   Combinational Logic (SCQF level 5)

Acceptable performance in this Unit will be the satisfactory achievement of the standards set out in this part of the Unit Specification. All sections of the statement of standards are mandatory and cannot be altered without reference to SQA.

OUTCOME 1

Verify the functions and characteristics of logic gates.

Performance Criteria

(a) Verify correctly the logic functions of AND, OR, and NOT gates.
(b) Verify correctly the logic functions of NAND, NOR, XOR gates.
(c) Verify correctly the electrical characteristics of a logic family.

OUTCOME 2

Investigate a combinational logic circuit.

Performance Criteria

(a) Correctly develop the truth table for a given logic expression.
(b) Correctly draw a combinational logic circuit for a given logic expression.
(c) Pin-assign the logic circuit correctly to Integrated Circuit (IC) packages.
(d) Correctly construct logic circuit on prototyping board for a given logic expression.
(e) Correctly test the operation of the logic circuit in relation to the theoretical truth table.

OUTCOME 3

Investigate combinational logic circuits to perform numerical operations.

Performance Criteria

(a) Correctly perform hexadecimal, decimal and binary conversion.
(b) Perform binary addition correctly.
(c) Construct and test a 2 input Half Adder (HA) cell using XOR and AND gates.

National Unit Specification: statement of standards (cont)

UNIT   Combinational Logic (SCQF level 5)

EVIDENCE REQUIREMENTS FOR THIS UNIT

Evidence is required to demonstrate that candidates have achieved all Outcomes and Performance Criteria.

Performance evidence supplemented with an assessor observation checklist as well as written and/or recorded oral evidence is required which demonstrates that the candidate has achieved all Outcomes to the standards specified in the Outcome and Performance Criteria.

This evidence should be produced under supervised, controlled conditions at appropriate points throughout the Unit either on an Outcome by Outcome basis or as integrated assessments. All calculations and measurements should be given using the relevant SI units of measurement.

The required evidence, for all Outcomes, is as follows:

For Outcome 1:

♦   correctly drawn and Pin assigned Logic Gate test arrangement
♦   accurate Logic Gate Truth Table test specification
♦   correctly constructed Logic Gate test arrangement
♦   accurate Logic Gate test results
♦   correct description of operation of Logic Gate

For PC (c) the limits of the following electrical characteristics should be correctly recorded:

♦   supply voltage V_{cc} for TTL and V_{dd} for CMOS
♦   voltage level for logic 0 for TTL and CMOS
♦   voltage level for logic 1 for TTL and CMOS

For Outcome 2:

♦   correctly drawn Layout Diagram
♦   correctly Pin assigned circuit diagram
♦   correctly constructed Logic Circuit
♦   accurate Logic Circuit Truth Table test specification
♦   accurate Logic Circuit test results
♦   correct description of operation of Logic Circuit

National Unit Specification: statement of standards (cont)

UNIT   Combinational Logic (SCQF level 5)

For Outcome 3:

♦ correctly performs hexadecimal, decimal and binary conversion for 4 bits
♦ correctly performs binary addition of two 4-bit binary words
♦ correctly interpreted XOR gate as SUM of the binary addition of two bits
♦ correctly interpreted AND gate as CARRY out of the binary addition of two bits
♦ correctly Pin assigned circuit diagram for Half Adder cell
♦ correctly drawn Layout Diagram for Half Adder cell
♦ correctly constructed Logic Circuit for Half Adder cell
♦ accurate Logic Circuit Truth Table test specification
♦ accurate Logic Circuit test results
♦ correct description of operation of Half Adder cell

The Assessment Support Pack for this Unit provides sample assessment material. Centres wishing to develop their own assessments should refer to the Assessment Support Pack to ensure a comparable standard.

National Unit Specification: support notes

UNIT   Combinational Logic (SCQF level 5)

This part of the Unit Specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

GUIDANCE ON THE CONTENT AND CONTEXT FOR THIS UNIT

This is a restricted core Unit within the National Certificate in Electronic Engineering at SCQF level 5 and can also be delivered as a free-standing Unit. The verification exercise for Outcome 1 PC(a) could be achieved by setting a single investigation involving one gate/inverter from IC packages 7408, 7432 and 7404 or their CMOS equivalents each being connected to common A, B inputs. Each function output from the AND, OR, and NOT gate can then be recorded on a single truth table with a column for each output. Similarly PC(b) may be developed using a second exercise comprising one gate from IC packages 7400, 7402 and 7486 or their CMOS equivalents each being connected to common A, B inputs. Each function output from the NAND, NOR, and EXOR gate is recorded on a second truth table with a column for each gate output. Both IEC/BS3939 and ANSI logic symbols should be introduced but all further work should be consistent within one standard.

Two input gates can be developed into 3-input and 4-input functions by combining 2-input gates, the resulting truth tables developed and compared with the 3-input or 4-input gate devices.

The investigation of the electrical characteristics of logic gates in PC(c) can focus on the logic families being used for investigation in Outcomes 1 and 2 eg LS, CMOS, HCT, HC etc. where the voltage levels associated with V_{cc} (5V) and V_{dd} (eg 6, 9, or 12V) supply and the low - Logic 0 state and the high — Logic 1 state are recorded and the limits of each level noted.

Sufficient formative exercises should be carried out for the candidate to develop the necessary expertise to achieve Performance Criteria (a) to (e) of Outcome 2. The formative exercises could be paper based for PC (a), (b) and (c) to give sufficient practice at drawing the combinational logic circuit from a given Boolean expression, developing the trugth for PC (a) and Pin-assigning the circuit for PC(c)

The bulk of the formative construction exercises for PC(d) could initially be developed using breadboard or some other pluggable non soldered logic tutor however some formative circuits should be built on prototyping board before moving on to the summative exercise; construction using prototyping board.

All the above activities, including the test results of the combinational logic circuits operation against the developed truth table should be recorded in the candidate's workbook and observational checklist.

National Unit Specification: support notes (cont)

UNIT   Combinational Logic (SCQF level 5)

For Outcome 3 it may be preferable that the investigation of number systems be made relevant to the hardware and techniques of digital systems, rather than a purely mathematical exercise. This can be introduced at appropriate times throughout the Unit. For example as an introduction to the Unit comparison can be made between the Decimal/Denary and Binary Number systems, later on when truth tables are introduced the column headings can be labelled using the base and radix of the binary number system this can then be used as an introduction to base conversion comparing row term values with binary values. Base 16 can be introduced as a compact way of representing long binary strings of 0's and 1's. MSI devices can be used to illustrate the conversion between denary to binary and binary BCD and binary to HEX etc. For PC(c) the arithmetic interpretation of the XOR gate and AND gate can be investigated alongside the arithmetic operation of binary addition in PC(b).

GUIDANCE ON LEARNING AND TEACHING APPROACHES FOR THIS UNIT

The approach to learning and teaching in this Unit is through practical investigation, discussion and demonstration. A workbook should be kept where the candidate records the results of their investigations and conclusions; hence indicating their progress and providing a record of activities carried out. The workbook should also clearly indicate exercises that are of sufficient merit to count towards summative assessment. The workbook should also demonstrate the full range of work carried out, both good and bad that has contributed to the candidates understanding.

The workbook could contain device pin-out diagrams, pin assigned circuit diagrams, construction layout diagrams, extracts from relevant datasheets etc. All relevant construction details and test methods used for each device and circuits investigated could be included along with candidate's descriptions of device/circuit operations.

A record of successfully completed test specifications for each circuit and device specified in the Performance Criteria should be included in the workbook.

Candidates should be encouraged to discuss between themselves how the basic gates operate and have time to build and investigate the operation of the logic gates before going on to investigate how to connect them together as combinational logic circuits.

OPPORTUNITIES FOR CORE SKILL DEVELOPMENT

The ability to interpret, convert, apply and produce data in diagram form underpins the competencies developed in the Unit. *Numeracy* skills will be naturally enhanced. Formative activities should be designed to increase confidence and familiarity with the practical interpretation, use and presentation of number and graphics in electronic engineering.

All elements of the Core Skill of *Problem Solving*, that is, Critical Thinking, Planning and Organising, reviewing will be developed as candidates plan and undertake investigations, construct circuits and test the operation. Although candidates have to demonstrate practical skills independently, group discussion, with assessor feedback, would support reflective review and evaluation of achievement.

UNIT Combinational Logic (SCQF level 5)

GUIDANCE ON APPROACHES TO ASSESSMENT FOR THIS UNIT

Opportunities for the use of e-assessment

E-assessment may be appropriate for some assessments in this Unit. By e-assessment we mean assessment which is supported by information and communications technology (ICT), such as e-testing or the use of e-portfolios or e-checklists. Centres which wish to use e-assessment must ensure that the national standard is applied to all candidate evidence and that conditions of assessment as specified in the Evidence Requirements are met, regardless of the mode of gathering evidence. Further advice is available in *SQA Guidelines on Online Assessment for Further Education (AA1641, March 2003), SQA Guidelines on e-assessment for Schools (BD2625, June 2005)*.

The required evidence can be generated throughout by means of practical investigation/assignments covering all three Outcomes developed over the course of the Unit. The activities carried out during the practical investigation/assignments being recorded in the workbook. With a folio of representative work selected from the workbook being submitted near the end with sufficient time for feedback and remediation.

All practical investigations for Outcome 1 Performance Criteria (a), (b) and (c) could be built on breadboard, progress and results being recorded in the candidate's workbook and on an observational checklist.

The practical investigation for Outcome 2 could be built on stripboard or similar, progress and results being recorded in the candidate's workbook and on an observational checklist.

For Outcome 3 Performance Criteria (a) and (b) an assignment could be set to guide the student through the investigation of number systems. For Performance Criteria (c) a practical investigation/assignments would cover the use of logic gates to implement binary addition circuits.

DISABLED CANDIDATES AND/OR THOSE WITH ADDITIONAL SUPPORT NEEDS

The additional support needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments, or considering whether any reasonable adjustments may be required. Further advice can be found on our website **www.sqa.org.uk/assessmentarrangements**