Course report 2023

National 5 Practical Electronics

This report provides information on candidates' performance. Teachers, lecturers and assessors may find it useful when preparing candidates for future assessment. The report is intended to be constructive and informative, and to promote better understanding. You should read the report in conjunction with the published assessment documents and marking instructions.

The statistics in the report were compiled before any appeals were completed.

Grade boundary and statistical information

Statistical information: update on courses

Number of resulted entries in 2022: 565

Number of resulted entries in 2023: 685

Statistical information: performance of candidates

Distribution of course awards including minimum mark to achieve each grade

A	Number of candidates	281	Percentage	41	Cumulative percentage	41	Minimum mark required	49
B	Number of candidates	160	Percentage	23.4	Cumulative percentage	64.4	Minimum mark required	42
C	Number of candidates	151	Percentage	22	Cumulative percentage	86.4	Minimum mark required	35
D	Number of candidates	49	Percentage	7.2	Cumulative percentage	93.6	Minimum mark required	28
No award	Number of candidates	44	Percentage	6.4	Cumulative percentage	100	Minimum mark required	N/A

Please note that rounding has not been applied to these statistics.

You can read the general commentary on grade boundaries in the appendix.

In this report:

- ‘most’ means greater than 70%
- ‘many’ means 50% to 69%
- ‘some’ means 25% to 49%
- ‘a few’ means less than 25%

You can find more statistical reports on the statistics and information page of SQA’s website.

Section 1: comments on the assessment

Question paper

The requirement to complete the question paper was removed for session 2022-23.

Practical activity

The practical activity performed as expected across the bank of four tasks which centres can select from. Each task is similar in complexity and provide sufficient opportunity for candidates to demonstrate different levels of performance from analysis and design through to build test and final reporting.

Regardless of the task chosen, or the experience of the assessor, candidates did well at certain stages and found other stages of the practical activity challenging. In all tasks, candidates found creating circuit layout diagrams, creating test plans and final circuit analysis challenging. The more practical, less reflective tasks, such as circuit simulation and construction, were done reasonably well by candidates.

Section 2: comments on candidate performance

Question paper

The requirement to complete the question paper was removed for session 2022-23.

Practical activity

Similar to previous years, candidates performed well in the more practical aspects of the task. These consisted of circuit construction, wiring and assembly as well as circuit simulation. This accounts for 51 marks of the available 70. In some instances, however, candidates did not follow the correct wiring convention for the construction of each sub-system. Where wiring conventions were followed, this helped candidates during circuit construction to identify faults during testing and repair.

The standard of soldering observed during verification visits was noted to be of an excellent standard, which is encouraging.

The analysis and design, testing and reporting stages of the practical activity are grade A skills, with candidates again finding these stages challenging. Costing and component lists in general were not well done. For a detailed list of components, there should be a table with a list of components, serial code, number of components, supplier, unit price and total price. To work out the total price of each type of component, candidates should investigate the price for a batch of components rather than multiplying the unit price by the number of components.

Section 3: preparing candidates for future assessment

Question paper

This course will return to full assessment requirements from session 2023-24 onwards. Please refer to the course specification for more information on the course assessment structure.

Centres may find the following key messages, which come from the 2019 course report, useful for preparing candidates for the return of this assessment.

- Candidates answering questions which require either restricted or extended responses should be wary of over-elaboration. Some candidates could identify errors in simulations but could not express themselves with the required degree of clarity or precision to gain the mark.
- Centres should ensure that candidates can describe, in a succinct and precise way, how to use the various instruments described in the course specification. In terms of applying relationships, candidates found calculating the reference voltage of a LM741 comparator very challenging and may need more practice in voltage division in general.
- Candidates need to be able to explain how a comparator and a transistor-controlled circuit works. Many candidates did not fully understand the relationship between voltage and resistance in a series circuit. Most candidates are now aware that when they are asked to draw circuit diagrams, they should ensure that there is a node on the end of the V+ and 0V lines.
- Candidates need to be aware of both types of bi-polar transistors (pnp as well as npn) and how these are positioned in simulations and circuit diagrams.
- Centres should be aware that most typical 'A type' questions are those which require the candidate to take information from one conceptual format and present it in another, for example, in block diagrams or when transferring a layout diagram to a circuit diagram (or vice versa).

Useful resources

- National 5 Practical Electronics – question paper understanding standards materials (this resource has examples of candidate evidence with commentaries)

Practical activity

It is essential that candidates have access to a suitable range of properly maintained tools and equipment and are given suitable guidance in order to achieve these tasks. Candidates will need to gain experience of using these tools and equipment, as well as the simulation software.

There are various websites that will assist assessors with the conventions used in the practical application of electronics such as circuit layout, test points, labelling components, as well as giving practical advice on how to develop good soldering skills.

Analysis and design:

- Candidates may benefit from compiling the components list from the simulation, and when they reach the construction phase they can go back to the listing and add components such as the 8 and 14 way DIL sockets for example. If such an approach is adopted, this would mean that the component list would be marked at the end of the construction phase.
- Candidates should be made aware that bill of materials should include an 'item ID' (R1, R2, LED 1, IC1, TR1, BZ1 etc). The item ID should be carried through to the Yenka simulation, breadboard planning, stripboard (layout) planning and testing.

Designing and simulating a solution:

- In most instances, candidates who struggled to produce a strip-board layout, were correctly provided with a fully annotated solution to use for circuit construction. This allowed candidates without a fully working layout diagram the opportunity to access all marks in the later construction stage.
- Yenka simulations should be clearly sectioned off and labelled with input, process and output.
- Layout diagrams should include all interconnections and track cuts. Layout diagrams should be created using the actual footprint of each component and not the simulation circuit symbol.
- It is good practice for test points to be planned and included in the layout diagram. Doing so should help candidates with the later testing stage.

Constructing the solution:

- The actual circuits built should replicate the layout diagrams to ensure consistency, but it may be necessary to make changes such as axial capacitors becoming radial capacitors due to components ordering.
- The stripboard plans and physical circuit should match exactly.
- It is good practice not to solder an IC onto a stripboard as it may damage the components inside it. A dual-in-line holder should be soldered first.
- Wiring conventions should be used. Red wires should only be used for power connections, both on the individual boards and in the loom. Black wires should only be used for ground connections. Any other colour of wire can be used for signals. There should always be three colours of wire. If red and black are not available, document using two other colours. The two chosen colours cannot therefore be used for any signal wiring.
- Professional circuit labelling kits can be purchased in order to prevent candidates using a marker pen to label stripboards. The colour of wiring used should reflect industrial practice, and not just what is available.
- Input, process and output boards should be easily disconnected from each other using either crimp connectors or terminal blocks in the wiring looms.

Testing the solution:

- Candidates should be encouraged to present three different test plans; pre-testing each sub-system, power testing each sub-system and power testing the three sub-systems connected together.
- Candidates will benefit from access to consumables that allow the insertion of fixed test points at circuit nodes that tie into their test plans. This aids candidates when taking measurements during testing and making subsequent repairs.
- Its good practice for pre-power-up checks to be in a table instead of written as paragraphs.
- Candidates should use a logic probe for testing, instead of a multimeter set on voltage.

Reporting on the solution:

- Centres may wish to provide candidates with a simple pro forma to record their progress through the practical activity, documenting activities they completed and what steps were next. Please refer to understanding standards resources for examples.
- Candidates would benefit from recording test results using bullet points or pin a table, instead of writing long paragraphs.

Useful resources

- National 5 Practical Electronics — practical activity case study: good practice (this resource highlights good practice from candidates and centres)
- National 5 Practical Electronics — Practical Electronics audio presentations (this resource covers each stage of the practical activity and supports the assessor's interpretation and application of the marking instructions)

Appendix: general commentary on grade boundaries

SQA's main aim when setting grade boundaries is to be fair to candidates across all subjects and levels and maintain comparable standards across the years, even as arrangements evolve and change.

For most National Courses, SQA aims to set examinations and other external assessments and create marking instructions that allow:

- a competent candidate to score a minimum of 50% of the available marks (the notional grade C boundary)
- a well-prepared, very competent candidate to score at least 70% of the available marks (the notional grade A boundary)

It is very challenging to get the standard on target every year, in every subject at every level. Therefore, SQA holds a grade boundary meeting for each course to bring together all the information available (statistical and qualitative) and to make final decisions on grade boundaries based on this information. Members of SQA's Executive Management Team normally chair these meetings.

Principal assessors utilise their subject expertise to evaluate the performance of the assessment and propose suitable grade boundaries based on the full range of evidence. SQA can adjust the grade boundaries as a result of the discussion at these meetings. This allows the pass rate to be unaffected in circumstances where there is evidence that the question paper or other assessment has been more, or less, difficult than usual.

- The grade boundaries can be adjusted downwards if there is evidence that the question paper or other assessment has been more difficult than usual.
- The grade boundaries can be adjusted upwards if there is evidence that the question paper or other assessment has been less difficult than usual.
- Where levels of difficulty are comparable to previous years, similar grade boundaries are maintained.

Grade boundaries from question papers in the same subject at the same level tend to be marginally different year on year. This is because the specific questions, and the mix of questions, are different and this has an impact on candidate performance.

This year, a package of support measures was developed to support learners and centres. This included modifications to course assessment, retained from the 2021–22 session. This support was designed to address the ongoing disruption to learning and teaching that young people have experienced as a result of the COVID-19 pandemic while recognising a lessening of the impact of disruption to learning and teaching as a result of the pandemic. The revision support that was available for the 2021–22 session was not offered to learners in 2022–23.

In addition, SQA adopted a sensitive approach to grading for National 5, Higher and Advanced Higher courses, to help ensure fairness for candidates while maintaining

standards. This is in recognition of the fact that those preparing for and sitting exams continue to do so in different circumstances from those who sat exams in 2019 and 2022.

The key difference this year is that decisions about where the grade boundaries have been set have also been influenced, where necessary and where appropriate, by the unique circumstances in 2023 and the ongoing impact the disruption from the pandemic has had on learners. On a course-by-course basis, SQA has determined grade boundaries in a way that is fair to candidates, taking into account how the assessment (exams and coursework) has functioned and the impact of assessment modifications and the removal of revision support.

The grade boundaries used in 2023 relate to the specific experience of this year's cohort and should not be used by centres if these assessments are used in the future for exam preparation.

For full details of the approach please refer to the National Qualifications 2023 Awarding — Methodology Report.