SQA Advanced Unit Specification

General information for centres

Unit title: Microprocessor and Microcontroller Technology

Unit code: HT1F 48

Unit purpose: This Unit is designed to enable candidates to recognise and understand Microprocessor and Microcontroller technology. It also provides the candidate the Opportunity to develop the knowledge and skills to program, test and interface memory devices.

On completion of the Unit candidates should be able to:

1. Analyse Microprocessor and Microcontroller architecture and operations
2. Outline the structure and use of memory devices
3. Program, test and interface a memory device

On completion of the Unit the candidate should be able to:

Credit value: 1 SQA Credit at SCQF level 8: (8 SCQF credit points at SCQF level 8*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from National 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should have a basic knowledge and understanding of computer architecture and programming. This may be evidenced by possession of a National Qualification Unit; Computing in Engineering. Or SQA Advanced Units. High level Engineering Software or MCU/MPU Assembly Language Programming. Possession of the SQA Advanced Unit MSI Devices would also help to enhance candidates' knowledge and understanding of the subject matter in this Unit.

Core skills: There may be opportunities to gather evidence towards Core Skills in this Unit, although there is no automatic certification of Core Skills or core skills components.

Context for delivery: This Unit was developed for the SQA Advanced Certificate/Diploma in Electronics awards. If this Unit is used in another group award(s) it is recommended that it should be taught and assessed within the context of the particular group award(s) to which it contributes

General information for centres

Unit title: Microprocessor and Microcontroller Technology

Assessment: The assessment of the first two Outcomes should be combined together into one assessment.

This paper should be taken by candidates at one single assessment event, lasting two hours. The assessment paper could be composed of a suitable balance of short answer, restricted response and structured questions. Assessment should be conducted under controlled, supervised conditions. It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

Outcome three should be assessed independently during a controlled practical laboratory assignment which should last one hour.

SQA Advanced Unit Specification: Statement of standards

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The sections of the Unit stating the Outcomes, knowledge and/or skills, and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Analyse Microprocessor and Microcontroller architecture and operation.

Knowledge and/or skills

- Microprocessor architecture and operation
- Microcontroller architecture and operation
- Address/control/data busses
- ALU's
- Instruction/accumulator/status/condition code/ flag registers
- CPU
- Input/output
- Program counter
- Address decoding
- Timing and control
- Memory maps/memory
- Interrupts

Evidence requirements

Evidence for knowledge and/or skills in this Outcome will be provided on a sample basis. The evidence may be presented in response to specific questions. Each candidate will need to demonstrate that she/he can answer questions correctly based on a sample of the items shown above. In any assessment, Microprocessor and Microcontroller architecture and operation must be assessed along with five out of the remaining ten knowledge and/or skills items.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a different sample of five from ten knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all seven items.

Where sampling takes place, a candidate's response can be judged to be satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

- explain the basic operation and characteristics of a Microprocessor
- explain the basic operation and characteristics of a Microcontroller
- draw a block diagram showing how various busses interconnect the CPU, memory and I/O
- explain the purpose of the ALU
- explain the purpose of the various registers
- state the two basic functions of the CPU
- explain the purpose of input/output interfacing
- explain the purpose of the program counter
- draw a block diagram of address decoding circuit and briefly explain the operation
- explain the purpose of timing and control circuitry
- draw a memory map showing memory allocation in hexadecimal
- draw a flow chart of data transfer with an interrupt taking place

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment of this Outcome should be combined with Outcome 2 to form a single assessment paper, details of which are given under Outcome 2.

Outcome 2

Outline the structure and use of memory devices.

Knowledge and/or skills

- Memory allocation
- RAM (Static/Dynamic)
- ROM
- Epsom
- Eeprom(Nvram)
- Eeprom (FLASHrom)

Evidence requirements

Evidence for knowledge and/or skills in this Outcome will be provided on a sample basis. The evidence may be presented in responses to specific questions.

Each candidate will need to demonstrate that she/he can answer correctly questions based on a sample of the items shown above. In any assessment of this Outcome four out of the six knowledge and/or skills items should be sampled.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a different sample of four out of six knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all four items.

Where sampling takes place, a candidate's response can be judged to be satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

- explain the governing factors over memory availability
- explain the difference between static and dynamic RAM
- explain the characteristics and operation of ROM
- explain how an Eeprom is programmed and erased and state advantages and disadvantage of this type of device
- explain how an Eeprom is programmed and erased and state advantages and disadvantages of this type of device
- explain how a FLASH Eeprom is programmed and erased and state advantages and disadvantage of this type of device

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used to elicit candidate evidence may take the form of an appropriate balance of short answer, restricted response and structured questions.

The assessment of this Outcome should be combined with Outcome 1 to form a single assessment paper. The single assessment paper should be taken at a single assessment event lasting 2 hours and carried out under supervised, controlled conditions. Such a paper could be composed of an appropriate balance of short answer, restricted response and structured questions.

Outcome 3

Program, test and interface a memory device

Knowledge and/or skills

- Program memory devices — RAM (Dynamic/Static), Eprom, Eeprom(FLASH rom), Eeprom(Nvram)
- Interface a suitable memory device
- Test for data retention/pattern faults such as checker board and walking ones and zeros

Evidence requirements

Evidence for knowledge and/or skills in this Outcome will be provided by practical assignment work. The evidence may be presented in response to a specific problem based on the application of programming and interfacing and testing a memory device.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a randomly selected problem is required each time the Outcome is assessed. Candidates must provide a satisfactory response to the problem.

A candidate's response can be judged to be satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

- program and interface a suitable memory device
- test the memory device

Evidence should be generated through a practical assignment undertaken in controlled, supervised conditions.

Assessment guidelines

Methods used to elicit candidate evidence may take the form of a practical assignment with an appropriate record sheet of achievement.

The practical assessment should be taken as a single event lasting one hour and carried out under supervised, controlled conditions.

Administrative information

Unit code: HT1F 48

Unit title: Microprocessor and Microcontroller Technology

Superclass category: XL

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SQA acknowledges the valuable contribution that Scotland's colleges have made to the development of SQA Advanced Qualifications.

FURTHER INFORMATION: Call SQA's Customer Contact Centre on 44 (0) 141 500 5030 or 0345 279 1000. Alternatively, complete our Centre Feedback Form.

SQA Advanced Unit Specification: Support notes

Unit title: Microprocessor and Microcontroller Technology

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

This Unit has been written in order to allow candidates to develop knowledge, understanding and skills in the following areas:

1. Understanding the architecture and operation of Microprocessor and Microcontroller technology.
2. Understand the structure and the use of memory devices.
3. Programming, interfacing and testing a memory device.

In designing this Unit the Unit writers have identified the range of topics they would expect to be covered by the lecturers. The writers have also given recommendations as to how much time should be spent on each Outcome. This has been done to help lecturers to decide what depth of treatment should be given to the topics attached to each of the Outcomes. While it is not mandatory for centres to use the list of topics it is strongly recommended that they do so to ensure continuity of teaching and learning across the Unit.

A list of topics is given below. Lecturers are advised to study this list of topics carefully before they commence the delivery of the Unit.

Outcome 1
Analyse microprocessor and microcontroller architecture and operations (20 Hours)

- architecture and characteristics of Microprocessors and Microcontrollers
- the component parts of Microprocessors and Microcontrollers
- bus connections between the various devices
- the function of the ALU
- the Logic functions AND, OR, NOT and exclusive OR
- accumulator register and its purpose
- the status register, the type of information contained within it and the main purpose of this register
- the condition code register and its relationship to the ALU
- the purpose of the flag register
- the contents and purpose of the instruction register
- CPU and how it executes arithmetic and logic operations. The type of data it can handle and the various control functions it carries

- input and output organisation.The purpose of I/O interfaces
- I/O device addressing - memory mapped port addressing and dedicated port addressing
- operation and purpose of the program counter
- address decoding and the use of a 2 to 4 line decoder. Operation of output enable, write enable, chip select used to read and write information to several devices within the system
- devices such as timer counter chip, input output chip
- the purpose of the timing and control circuits
- memory organisation within the system including the description of the concept of the memory map showing allocation of various groups of memory to areas such as the operating system ROM, software language ROM, video display RAM, user RAM, operating system RAM
- the use of interrupts

Outcome 2
Outline the structure and use of memory devices (7 hours)

- the factors which govern the size of the memory available
- the volatility of RAM and ROM and how loss of data can be prevented
- the use to which RAM and ROM are put to, the flexibility of these devices
- the relevance to power and space with static and dynamic RAM
- the difference between mask ROM and PROM
- equipment used to program and erase an Eprom
- the advantages and disadvantages of Eeprom and Eeprom
- the features of FLASH Eeprom and their advantages

Outcome 3
Program, test and interface a memory device (10 Hours)

Assessment 3 hours

Guidance on the delivery and assessment of this Unit

It should be noted that this Unit can be delivered on a freestanding basis or can be used alongside the programming (assembly or high level) language Units.

This Unit should be assessed by one assessment paper lasting 2 hours for Outcomes 1 and 2 which should take place at the end of the Unit prior to a practical assignment covering the requirements of Outcome 3 and lasting 1 hour.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of on line support. However with regards to the assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence.

Arrangements would be required to be put in place to ensure that assessment whether done at a single or at multiple events was conducted under controlled, supervised conditions.

To keep administrative arrangements to a minimum, it is recommended that a single assessment paper (taken by candidates at a single assessment event) be used for distance learning for Outcomes 1 and 2 however a separate practical assignment under controlled, supervised conditions will also be necessary.

For information on normal open learning arrangements, please refer to SQA guide *Assessment and Quality Assurance of Open and Distance Learning (SQA 2000).*

Equality and inclusion

This Unit specification has been designed to ensure that there are no unnecessary barriers to learning or assessment. The individual needs of learners should be taken into account when planning learning experiences, selecting assessment methods or considering alternative evidence.

Further advice can be found on our website www.sqa.org.uk/assessmentarrangements.

General information for candidates

Unit title: Microprocessor and Microcontroller Technology

This Unit has been designed to allow you to develop knowledge, understanding and skills in microprocessor architecture and memory devices.

The precise form the assessment will take will depend on the centre where you are taking the Unit. However, Outcomes 1 and 2 will be assessed at one assessment event and Outcome 3 at a practical event. The assessment of Outcomes 1 and 2 combined will take place at the end of the Unit, will comprise of one assessment paper lasting two hours and will take place under supervised, controlled conditions. The assessment will be conducted under closed book conditions in which you will not be allowed to take notes, textbooks etc into the assessment.

Outcome 3 will be assessed after completion of Outcomes 1 and 2 combined assessment. It will be carried out as a practical assignment under supervised, controlled conditions.