SQA Advanced Unit specification

General information for centres

Unit title: Digital Electronics

Unit code: HT7L 47

Unit purpose: The Unit is designed to enable candidates to know, understand and apply the basic concepts of digital electronics. It provides candidates with an opportunity to develop the knowledge and skills to be able to design and construct logic circuits to meet a design brief.

On completion of the Unit candidates should be able to:

1 Produce truth tables and associated Boolean expressions for logic gates.
2 Design combinational logic circuits using minimisation techniques.
3 Describe the operation of sequential logic circuits.
4 Construct logic circuits.

Credit points and level: 1 SQA Credit at SCQF level 7: (8 SCQF credit points at SCQF level 7*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from National 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should have a basic knowledge of digital electronic engineering. This may be evidenced by possession of the following National Qualification courses: C027 12 Electronics, C025 11 Electronic and Electrical Fundamentals at Intermediate 2 or the following National Qualification Units: E9S3 04 *Combinational Logic*, E9SG 12 *Sequential Logic* and E9SB *12 Logic Families and Digital System Analysis*. However, entry requirements are at the discretion of the centre.

Core Skills: There may be opportunities to gather evidence towards the following Core Skills or Core Skills components in this Unit. There is however no automatic certification of Core Skills or Core Skill components:

- Written Communication (reading) at National 5
- Using Number at National 4
- Using Graphical Information at National 5
- Using Information Technology at National 5
- Critical Thinking at National 5
- Working with Others at National 4

Context for delivery: This Unit has been developed for the SQA Advanced Diploma in Electrical Engineering Group Award. If this Unit is delivered as part of a Group Award, it is recommended that it should be taught and assessed within the subject area of the Group Award to which it contributes.

Assessment: The assessment for Outcomes 1, 2 and 3 in this Unit should be combined into one assessment paper. The paper should be taken by candidates at one single assessment event, which should last two hours. The assessment paper should be composed of a suitable balance of short answer, restricted response and structured questions. Assessment should be conducted under controlled, supervised conditions.

Outcome 4 should be assessed by a circuit building exercises lasting a total of two hours.

It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

SQA Advanced Unit specification: statement of standards

Unit title: Digital Electronics

Unit code: HT7L 47

The sections of the Unit stating the Outcomes, knowledge and/or skills, and Evidence Requirements are mandatory. Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Produce truth tables and associated Boolean expressions for logic gates.

Knowledge and/or skills

- hexadecimal number system
- conversion between binary and hexadecimal numbers
- conversion between hexadecimal and binary numbers
- Gate symbols
- Truth tables and associated Boolean expression for AND/OR/NOT/EXOR/NAND and NOR gates

Outcome 2

Design combinational logic circuits using minimisation techniques.

Knowledge and/or skills

- combinational logic expressions in sum of products (S of P) and product of sums (P of S) forms
- minimise expressions using Boolean algebra
- draw Karnaugh maps
- use Karnaugh maps to minimise logic expressions
- draw minimised circuit diagrams

Outcome 3

Describe the operation of sequential logic circuits.

Knowledge and/or skills

- difference between combinational and sequential logic
- block diagram of sequential machine
- need for feedback and memory in sequential logic
- cross coupled SR latch circuit
- JK and D bistable elements
- clock signals and edge triggering
- asynchronous and synchronous operations
- counter and shift register circuits using bistables

Outcome 4

Construct logic circuits.

Knowledge and/or skills

- logic family device characteristics
- circuit construction methods
- select the appropriate gate elements to construct logic circuits
- SR latch operation
- build and test counters and shift register circuits

Evidence Requirements for Outcomes 1, 2 and 3

Evidence for the knowledge and/or skills in Outcomes 1, 2 and 3 will be provided on a sample basis. The evidence may be presented in responses to specific questions. Each candidate will need to demonstrate that she/he can answer correctly questions based on a sample of the items shown under the knowledge and skills items in the Outcomes. In any assessment of the Outcomes **three out of five** knowledge and/or skills items should be sampled from Outcome 1, **three out of five** knowledge and/or skills items from Outcome 2 and **five out of eight** knowledge and/or skills items from Outcome 3.

In order to ensure that candidates will not be able to foresee what items they will be questioned on, a different sample of three out of five knowledge and/or skills items from Outcome 1, three out of five knowledge and/or skills items from Outcome 2 and five out of eight knowledge and/or skills items from Outcome 3 are required each time the Unit is assessed. Candidates must provide a satisfactory response to all items.

Where sampling takes place, a candidate's response can be judged to be satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

Outcome 1

- convert two binary numbers to hexadecimal showing all working
- convert two hexadecimal numbers to binary showing all working
- draw current gate symbol for three different logic gates
- draw the truth table for three different logic gates
- derive the associated Boolean expression for three different logic gates

Outcome 2

- write two combinational logic expressions in sum of products (S of P) form
- write two combinational logic expressions in product of sums (P of S) form
- use Boolean algebra to minimise two, three input variable expressions
- draw and use Karnaugh maps to minimise one, four input variable S of P expression
- draw circuit diagrams to implement two logic expressions

Outcome 3

- explain the difference between combinational and sequential logic
- draw the block diagram of a sequential machine
- draw the circuit diagram of an SR latch using cross coupled NAND or NOR gates

- derive the state table for an SR and a JK bistable (flip-flop)
- draw the circuit symbol an edge triggered JK and a D bistable
- sketch the waveform generated by a train of six clock pulses and show three positive and three negative edge triggered signals
- explain the difference between asynchronous and synchronous operations
- draw the bistable based circuit diagrams for both a counter or shift register

Evidence should be generated through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed-book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment. Candidates will be permitted to use scientific calculators during the assessment.

Assessment guidelines for Outcomes 1 to 3

The assessment for Outcomes 1 to 3 should be combined to form one assessment paper. This assessment paper should be taken at a single assessment event, lasting two hours, and carried out under supervised, controlled conditions. Such a paper should be composed of an appropriate balance of short answer, restricted response and structured questions.

Evidence Requirements for Outcome 4

Evidence of knowledge and skills can be demonstrated by the candidate:

- selection of devices
- verifying the operation of a pre-constructed SR latch
- construct and test:
  - a four input combinational logic circuit having a minimum of six gates
  - a MOD eight counter OR a three stage serial shift register
- maintaining a log showing the circuit diagram, devices used, layout diagram, input/output signals and test results

Assessment guidelines for Outcome 4

The candidate should be provided with a construction kit, device data sheets and a written specification of the circuits to be built. The assessment lasting two hours should be undertaken under in controlled supervised conditions and be presented as a written report along with the artefacts produced.

Administrative information

Unit code: HT7L 47

Unit title: Digital Electronics

Superclass category: XL

Date of publication: August 2017

Version: 01

History of changes

Version	Description of change	Date

Source: SQA

SQA acknowledges the valuable contribution that Scotland's colleges have made to the development of SQA Advanced qualifications.

FURTHER INFORMATION: Call SQA's Customer Contact Centre on 44 (0) 141 500 5030 or 0345 279 1000. Alternatively, complete our Centre Feedback Form.

SQA Advanced Unit specification: support notes

Unit title: Digital Electronics

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

The Unit has been written in order to allow candidates to develop knowledge, understanding and skills in the following areas:

1 Produce truth tables and associated Boolean expressions for logic gates.
2 Design combinational logic circuits using minimisation techniques.
3 Describe the operation of sequential logic circuits.
4 Constructing logic circuits.

This Unit has been developed to introduce candidates on the SQA Advanced Diploma in Electrical Engineering to digital electronics.

In designing this Unit, the writers have identified the range of topics expected to be covered by lecturers. They have also given recommendations as to how much time should be allocated to each Outcome. This has been done to help tutors to decide the depth of treatment which should be give to each topic within an Outcome. Whilst it is not mandatory for centres to use this list of topics, it is strongly recommended that they do so to ensure candidates have the adequate knowledge and skills needed by many employees in electronic, electrical, control and computer industries.

The following is a range of the topics covered in this Unit:

- the use of binary arithmetic in digital systems
- production of simple combinational logic expressions
- construction and testing of combinational logic circuits to meet given applications
- explanation of the differences between combinational and sequential logic
- sequential logic devices
- sequential logic circuit operations
- latch operations
- operation of SR, D, and JK bistables
- clock signals and their use in edge triggered bistables
- construction and testing counter and shift register circuits

A list of topics is given below. Lecturers are advised to study this list of topics so that they can get a clear indication of the standard of achievement expected of candidates in this Unit.

1 Produce truth tables, and associated Boolean expressions for logic gates. (4 hours)

- revision of decimal number system
- binary number system
- decimal/binary and vice versa conversion methods
- hexadecimal number system

- binary/hexadecimal and vice versa conversion methods
- current gate symbols for AND/OR/NOT/EXOR /NAND/NOR logic gates
- truth table and Boolean expression for each gate
- use logic tutor boards to verify gate signals

2 Design combinational logic circuits using minimisation techniques. (7 hours)

- write combinational logic expressions in Sum of Products (S of P) and Product of Sums (P of S) forms
- minimise expressions using Boolean algebra
- draw Karnaugh maps for S of P expressions
- minimise expressions by looping variables on a Karnaugh map
- draw logic circuit diagrams
- prove logic identities using truth tables

3 Describe the operation of sequential logic circuits. (12 hours)

- compare combinational and sequential logic
- memory in sequential logic
- clock signals
- asynchronous and synchronous operations
- SR latch operation
- verify the state tables for bistable devices
- edge triggering
- counter and shift register circuits using bistables

4 Construct logic circuits (14 hours)

- selection of devices
- circuit construction methods
- construct and test combinational logic circuits
- construct and verify the operation of cross coupled SR latch
- construct counter and shift register circuits
- use software to simulate and test circuits
- use test equipment

Unit assessment (4 hours)

A two hour written assessment having a balanced mix of short answer, restricted response and structured questions designed to elicit candidate knowledge.

A two hour practical exercise in which the candidate should build and test digital circuits.

Guidance on the delivery and assessment of this Unit

This Unit is a suitable introduction to digital electronic systems. The Unit has been designed to allow candidates sufficient time to carry out a range of practical experimentation, circuit construction and verification exercises to supplement their learning. Tutors should make available experimental exercises which will allow candidates, where possible, to work on their own. Candidates should have free access to manufacturer's data sheets for the devices used.

Computer simulation could form part of the teaching and learning process such as the verification of Boolean identities and Karnaugh mapping.

Details on approaches to assessment are given under Evidence Requirements and Assessment guidelines under each Outcome in the SQA Advanced Unit specification: statement of standards section. It is recommended that these sections be read carefully before proceeding with assessment of candidates.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of on-line support. Candidates will also require access to a centre which, can provide circuit construction facilities. With regard to assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence. Arrangements would be required to ensure that the evidence whether done at a single or at multiple events was conducted under controlled, supervised conditions.

Equality and inclusion

This Unit specification has been designed to ensure that there are no unnecessary barriers to learning or assessment. The individual needs of learners should be taken into account when planning learning experiences, selecting assessment methods or considering alternative evidence.

Further advice can be found on our website www.sqa.org.uk/assessmentarrangements.

General information for candidates

Unit title: Digital Electronics

This Unit has been designed to allow you to develop knowledge, understanding and skills associated with digital electronics which is the basis of digital control systems and computer technology.

The early part of the Unit deals with the basic elements of number systems and digital electronics and should provide you with a good grounding in this subject area. For those who have studied digital electronics in an earlier course this Unit will provide some opportunities for revision.

The Unit will enable you to understand digital electronic systems. On completion of the Unit you should be able to read and draw circuit diagrams containing standard digital devices. You should also be able to use computer software to simulate and test functionality prior to the construction of digital circuits.

By the end of the Unit you will be expected to explain combinational and sequential circuit operation and to construct digital circuits.

The final assessment will take the form of a short answer written test paper, lasting two hours, taken under supervised, controlled closed-book conditions. You will not be allowed to take notes, textbooks, etc, into the assessment. You will, however, have access to device data sheets. In order to allow you to show evidence of practical expertise, there will be a two-hour build and test exercise. This latter exercise is likely to be conducted in a laboratory at a different time from the written assessment.