SQA Advanced Unit Specification

General information for centres

Unit title: Interfacing Electronics

Unit code: HV45 47

Unit purpose: The purpose of this Unit is to give candidates an understanding of interfacing electronic circuits, which includes choice of components, problems to be overcome and the application of this knowledge to a multi-stage circuit.

On completion of the Unit the candidate should be able to:

1 Identify a range of passive and active electronic components.
2 Identify various load requirements and characteristics for a selection of electro-mechanical components and substrates and how they interface with electronic components.
3 Identify and analyse appropriate interface components to connect stages in a multi-stage circuit.
4 Investigate and analyse wireless and fibre optic interfacing techniques.

Credit points and level: 1 SQA Credit at SCQF level 7: (8 SCQF credit points at SCQF level 7*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from National 1 to Doctorates.*

Recommended prior knowledge and skills: It would be an advantage for candidates to have a basic knowledge and understanding of analogue and digital electronics, test instruments and testing skills. However entry requirements are at the discretion of the centre.

Core Skills: There may be opportunities to gather evidence towards the following listed Core Skill components in this Unit, although there is no automatic certification of Core Skills or Core Skills components.

Problem Solving	SCQF level 6
Using Information Technology	SCQF level 6
Numeracy	SCQF level 6

Context for delivery: If this Unit is delivered as part of a Group Award, it is recommended that it should be taught and assessed within the subject area of the Group Award to which it contributes.

Assessment: Outcomes 1 and 2 should take the form of a single assessment event lasting one hour and should be conducted under closed booked controlled, supervised conditions.

Outcome 3 is assessed by a practical exercise under controlled, supervised conditions, where the candidate will have access to electronic computer aided packages and data sheets and produce a report of 500 words minimum.

Candidates should complete this report in their own time.

Outcome 4 assessed through an investigation report of 500 words minimum and it is expected that the report will be written up in the candidates' own time.

Centres should make every reasonable effort to ensure the assignment solution is the candidate's own work. Where copying or plagiarism is suspected candidates may be interviewed to check their knowledge and understanding of the subject matter. A checklist should be used to record oral evidence of the candidate's knowledge and understanding.

SQA Advanced Unit specification: statement of standards

Unit title: Interfacing Electronics

Unit code: HV45 47

The sections of the Unit stating the Outcomes, knowledge and/or skills, and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Identify a range of passive and active electronic components.

Knowledge and/or skills

- Resistors
- Capacitors
- Inductors
- Diodes
- Transistors
- Opto-electronic devices
- Electronic switches
- Integrated Circuits

Evidence Requirements

Evidence for the knowledge and or skills in this Outcome will be provided on a sample basis. The evidence may be presented in response to specific questions.

In any assessment of Outcome 1, **two** components from **each** of the **eight** knowledge and/or skills items should be sampled. Students should be allowed access to data sheets.

In order to ensure that the candidates will not be able to foresee what items they will be questioned on, a different sample of **two** components from **each** of the **eight** knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all assessed items.

Where sampling takes place, a candidate's response can be satisfactory where evidence provided is sufficient to meet the requirements for each item by showing that the candidate is able to:

Identify with the aid of data sheets a range of passive and active components, their pin out and package types and mountings of two from each of the knowledge and/or skills listed below:

- Resistors
  - Carbon axial
  - Surface mount
  - Power
  - Variable

- Capacitors
  - Radial electrolytic
  - Tantalum
  - Surface mount
  - Polyester
  - Variable

- Inductors
  - Air
  - Ferrite
  - Iron
  - Surface mount

- Diodes
  - LED
  - Small signal
  - Photo-diode
  - Zener
  - Power diode
  - Bridge rectifier

- Transistors
  - BJT
  - FET
  - Power MOSFET

- Opto-electronic devices
  - Photo-transistor
  - Slotted opto-switch
  - DIL package

- Electronic switches
  - Thyristors
  - Triacs
  - Diac

- Integrated circuits
  - Timers
  - Counters
  - Logic gates
  - Amplifiers
  - Comparators

Assessment guidelines

Questions used to elicit candidates' evidence should take the form of appropriate balance of short answer, restricted response and structured questions. Candidates should be allowed access to data sheets.

The assessment of this Outcome should be combined with that for Outcome 2 to form a single assessment paper, details of which are given under Outcome 2.

Outcome 2

Identify various load requirements and characteristics for a selection of electro-mechanical components and substrates and how they interface with electronic components.

Knowledge and/or skills

- Loads
- Interfaces

Evidence Requirements

Evidence for the knowledge and or skills in this Outcome will be provided on a sample basis. The evidence may be presented in response to specific questions.

In any assessment of this Outcome **five** out of **nine** loads and **three** out of **five** interfaces above should be sampled.

In order to ensure that the candidates will not be able to foresee what items they will be questioned on, a different sample of **five** out of **nine** loads and **three** out of **five** interfaces in the knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all sampled items.

Each candidate will need to demonstrate that she/he can answer questions which:

- Identify various load requirements and characteristics for the selected electro-mechanical components and substrates.
- Select appropriate interface for a given load, characteristics or parameters.

- Loads
  - Relays
  - Contactors
  - Solid state
  - Visual indication
  - Audible indication
  - Motors
  - Transformers
  - Regulators
  - Solenoids

- Interfaces
  - Filters
  - Switches
  - Drivers
  - Protection
  - Substrates

Assessment guidelines

Outcomes 1 and 2 should take the form of a single assessment event lasting one hour and should be conducted under closed booked controlled, supervised conditions. Such a paper should compose of appropriate balance of short answer, restricted response and structured questions. Candidates should have access to data sheets.

Outcome 3

Identify and analyse appropriate interface components to connect stages in a multi-stage circuit.

Knowledge and/or skills

- Transistor based switching circuit
- Operational amplifier circuits (DIL)
- Combinational Logic Circuits
- Timer/Counter/Driver circuits
- Power supply circuits

Evidence Requirements

Evidence for the knowledge and or skills in this Outcome will be provided on a sample basis. The evidence may be presented in response to a practical or simulated assignment using a four stage circuit.

In any assessment of Outcome 3, **one** component from each of **five** knowledge and/or skills items above should be sampled.

In order to ensure that the candidates will not be able to foresee what items they will be questioned on, a different sample of **one** component from each of **five** knowledge and/or skills items is required each time the Outcome is assessed. Candidates must provide a satisfactory response to all assessed items.

Each candidate will need to demonstrate that she/he can

- Select the correct interfaces for a given four stage circuit
- Verify the correct operation of the completed four stage circuit.
- Produce a 500 word minimum report that will include:
  - Graphic information (eg circuit diagram, wave forms)
  - Calculations and test results
  - Discussion and conclusion

- Transistor based switching circuit
  - Opto-electronic
  - BJT
  - FET

- Operational amplifier circuits (DIL)
  - Inverting
  - Non-inverting
  - Voltage follower
  - Comparator.

- Combinational Logic Circuits
  - NOT
  - AND
  - NAND
  - OR
  - NOR

- Timer/Counter/Driver circuits
  - 555 timer
  - 4 Bit up/down counter
  - RS232/USB/Fibre optic
  - Programmable

- Power supply circuits
  - Unregulated
  - Regulated
  - Switched mode

Assessment guidelines

Evidence for this Outcome will be by a candidate undertaking a practical assignment on all knowledge and/or skills items.

Practical assignment will be carried out in a workshop or by computer simulation under controlled supervised conditions lasting 1 hour. Candidates should complete a report of 500 words minimum in their own time.

Centres should make every reasonable effort to ensure the assignment solution is the candidate's own work. Where copying or plagiarism is suspected candidates may be interviewed to check their knowledge and understanding of the subject matter. A checklist should be used to record oral evidence of the candidate's knowledge and understanding.

Outcome 4

Investigate and analyse wireless and fibre optic interfacing techniques

Knowledge and/or skills

- Wireless technology
- Fibre optic technology

Evidence Requirements

Evidence for this Outcome will be provided by a candidate undertaking an assignment of 500 words minimum based on a sample of **one** from **two** knowledge and/or skills items.

For the assignment the candidates must produce a report in their own time that must include:

- Briefly describe the of operation of wireless or fibre optic interfacing techniques which may include block diagrams and sketches
- Advantages and disadvantages of wireless or fibre optics versus traditional hardwired
- Typical Application

Assessment guidelines

This should take the form of an assignment of 500 words minimum. The intention of this Outcome is for the students to research techniques of interfacing. Interfacing takes place with wireless and optical technology, where the electronic pathway is replaced by another medium and recent personal computers are often interfaced to these technologies.

Candidates should complete the report in their own time.

Centres should make every reasonable effort to ensure the assignment solution is the candidate's own work. Where copying or plagiarism is suspected candidates may be interviewed to check their knowledge and understanding of the subject matter. A checklist should be used to record oral evidence of the candidate's knowledge and understanding.

Administrative Information

Unit code: HV45 47

Unit title: Interfacing Electronics

Superclass category: XL

Date of publication: November 2017

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Source: SQA

SQA acknowledges the valuable contribution that Scotland's colleges have made to the development of SQA Advanced Qualifications.

FURTHER INFORMATION: Call SQA's Customer Contact Centre on 44 (0) 141 500 5030 or 0345 279 1000. Alternatively, complete our Centre Feedback Form.

SQA Advanced Unit specification: support notes

Unit title: Interfacing Electronics

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

This Unit has been written to allow candidates to develop knowledge, understanding and skills in the following areas:-

1 Identify a range of passive and active electronic components.
2 Identify various load requirements and characteristics for a selection of electro-mechanical components and substrates and how they interface with electronic components.
3 Identify and analyse appropriate interface components to connect stages in a multi-stage circuit.
4 Investigate and analyse wireless and fibre optic interfacing techniques.

The purpose of this Unit is to provide candidates with an opportunity to acquire knowledge and understanding of the types and range of electronic components available for functionality and interfacing.

The candidate should be instructed in the use of a range measuring equipment. The multi-stage circuit produced should be tested and inspected to ensure compliance with the specification, and schematics. An evaluation should then be made of the fitness for purpose of the circuit. The assessor may issue pre-constructed circuits or simulation.

The Unit has been developed for the SQA Advanced Certificate/Diploma in Mechatronics framework.

The content reflects the need for candidates to select appropriate components, equipment and techniques to interface different circuits and the problems encountered with different electronic technologies.

It is not intended as a complete electronics Unit, but as an introduction to the problems and factors to be considered when electronic circuits are constructed and interfaced to another ‘stage’ or circuit.

Allocated delivery times are for guidance purposes only.

Outcome 1 (5 hours) — The aim of this outcome is for students to identify typical electronic components and the wide range operational parameters required for in-circuit operation. Passive and active components are identified in respect to their voltage, current and power requirements, with emphasis on the tolerances and limitations. This encompasses both mechanical and electrical connections. It is envisaged that extensive use of data books, software packs, data sheets and the Internet as well as the ability to use colour coded and numbering systems, will be required by candidates.

Typical information would that could be tabulated:

- Pin/Fan outs
- Mounting/package type
- Truth tables
- Timing
- Frequency
- Bandwidth/gain
- Voltage
- Current
- Power
- Resistance/impedance
- Capacitance
- Inductance

Outcome 2 (9 hours) — The aim of this Outcome is for students to understand the physical and electronic interfaces, input stage, main stage, and the output stages. Load calculations could be performed e.g. the current drawn from the supply, voltage dropped, and load current, ripple voltage. Verification should be performed by simulation or mathematical calculation used to authenticate.

The multi-stage circuit calculations should be applied to the all interfaces for each stage. The use of pre-constructed circuits with various loads could be used to enhance the candidates understanding and the following parameters and effects may be considered.

- Load Current
- Voltage drop
- Ripple voltage
- Starting current
- Voltage regulation
- Step up / down voltage
- Simple low pass filter limitations.
- Signal integrity (timing / clipping / saturation)
- Drivers (RS232 / USB / Fibre optic)
- Steady state switching of resistive and inductive loads
- Over current and voltage protection
- Track widths

Outcome 3 (19 hours) — The aim of this Outcome is to use the above knowledge and skills to insert the correct components into a four stage circuit. Pre-constructed circuits may be used to demonstrate the interfacing.

- Stage 1 (Power supply), Stage 2 (Switched input: Comparator/Timer/Counter), Stage 3 (digital circuit/opto switches), Stage 4 (Transistor driving relay to switch a suitable load)
- OR another suitable multi-stage circuit designated by the assessment centre.

Measurements of circuit parameters should be taken at each 'output stage' of individual stages to verify the functionality of the complete circuit. At least one of these should be graphical and all schematic circuit diagrams should show component identification and inter-connecting paths.

- Transistor based switching circuit
  - Opto-electronic
  - BJT
  - Fet

- Operational amplifier circuits (DIL)
  - Inverting
  - Non-inverting
  - Voltage follower
  - Comparator.

- Combinational Logic Circuits
  - NOT
  - AND
  - NAND
  - OR
  - NOR (CMOS/TTL)

- Timer/Counter/Driver circuits
  - 555 timer
  - 4 Bit up/down counter
  - RS232/USB/Fibre optic
  - Programmable

- Power supply circuits
  - Unregulated
  - Regulated
  - switched mode

The multi-stage (**4 stages minimum**) circuit will be pre-constructed or simulated circuits, accompanied by schematics, then simulated where the candidate will insert the correct components into the circuit and measurements recorded of inputs and outputs of each stage of the circuit. Written and graphical evidence will be required for each circuit interface and for the completed multi-stage circuit.

Outcome 4 (5 hours) — The aim of this Outcome is for students to examine modern interfacing techniques eg:

- Wireless technology interfacing
- Fibre-optic technology

This can take the form of an assignment based on research, with written and graphical information, such as block diagrams and their practical application.

The transmitter, the medium through which it travels and the receiver should be discussed for each technology and this should be related to practical examples, such as interfacing with personal computers. A report of 500 words minimum should be produced and block diagrams used to show the connectivity and communication paths

Guidance on the delivery and assessment of this Unit

This Unit should be delivered predominantly using practical exercises that will allow candidates to learn and develop knowledge and skills. The candidate will utilise a multi-stage circuit that demonstrates their competence in the skill range. The assessment of this Unit comprises of a written paper lasting 1 hour, which covers Outcomes 1 and 2. Outcome 3 is assessed by a practical exercise where a report will be produced of 500 words minimum. Outcome 4 is assessed through an investigation report of 500 words minimum.

Short answer questions will be required to ensure coverage of the knowledge and/or sections, and where appropriate multiple-response or multiple choice questions can be used for identification purposes. Allocated times are for guidance purposes only.

This Unit should be delivered by a combination of lecturing, group and individual working, and it is anticipated that circuits will be pre-constructed using the range of components or by simulation. The short answer questions may be required to ensure coverage of the knowledge skills area.

Opportunities for developing Core Skills

Candidates complete two practical investigations using electronic computer aided packages and data sheets. All elements of the Core Skill of Problem Solving, namely planning and organising, critical thinking, and reviewing and evaluating will be naturally developed and enhanced as the Unit is undertaken. Formative opportunities for interpretation and evaluation of a range of examples of graphic information and for practical working with wireless and optical technology would be of value. Discussions with the class group and/or the assessor on practical interfacing applications, such as interfacing with personal computers would reinforce evaluative and analytical skills.

As they investigate and analyse wireless and fibre optic interfacing techniques candidates could be encouraged to formally identify specific objectives and to review potential solutions to a number of associated theoretical and practical problems. The chance to identify and fully consider any underlying variables and to examine the relative significance of each before justifying and implementing an appropriate solution will provide opportunities to develop problem solving skills to an advanced level. Evaluation of the potential effect and impact of proposed solutions will be formally assessed in written reports. Candidates could be supported in identifying appropriate methods of reviewing and discussing the advantages and disadvantages of wireless or fibre optics versus traditional hardwired methods.

Accuracy in the interpretation and communication of graphic, testing and calculation information underpins the competencies developed in the Unit. Candidates will benefit from formative opportunities to further develop effectiveness in analysing and applying graphic and numerical data. Software packages or on-line tutorials to enhance existing skills may be useful. The emphasis of formative work should be on Numeracy as a tool to be used and applied efficiently and critically in electronics contexts.

Open learning

This Unit could be delivered by distance learning, which may incorporate some degree of online support. However, with regards to assessment, planning would be required by the centre concerned to ensure the sufficiency and authenticity of candidate evidence. Arrangements would be required to be put in place to ensure that assessment, whether done at a single or multiple events, was conducted under controlled, supervised conditions.

For information on normal open learning arrangements, please refer to the SQA guide *Assessment and Quality of Open and Distance Learning* (SQA 2000).

Equality and inclusion

This unit specification has been designed to ensure that there are no unnecessary barriers to learning or assessment. The individual needs of learners should be taken into account when planning learning experiences, selecting assessment methods or considering alternative evidence.

Further advice can be found on our website www.sqa.org.uk/assessmentarrangements.

General information for candidates

Unit title: Interfacing Electronics

This Unit has been designed to allow you to develop knowledge and understanding about the technical difficulties of interfacing a number of circuits to operate harmoniously with each other.

The Unit commences with a review of a wide range of electronic components, how to recognise them, how to source them, their characteristic tolerances and limitations, and their function.

However, when electronic components are interfaced in a circuit they are likely to be connected to a larger load at the output stage of the final circuit, therefore these components will tend to be bulkier and physically larger.

When interfacing any circuit there are electronic difficulties as well as physical. These could include the load current, power supply, protection, timing, how it is mounted, physical size, heat dissipation, and cooling. When the current/voltages/power consumption are calculated it allows the design of the circuit to be modified to overcome these difficulties.

Having understood the breadth of components the next exercise is to insert these components into a functional multi-stage circuit. The multi-stage circuit originates as a conceptual design with a block diagram then moves towards the schematic design. The multi-stage circuit will have a power supply, an input stage, the control/signal/conditioning stage and the output stage.

The end of the Unit asks you to investigate some modern interfacing techniques to help broaden your understanding that interfacing takes place with wireless and optical technology, where the electronic pathway is replaced by another medium. Block diagrams are acceptable for this Outcome.

The formal assessments for this Unit consist of an assessment paper covering Outcomes 1 and 2 lasting 1 hour. The assessment paper for Outcomes 1 and 2 will be conducted under closed book conditions, where you will have access to data sheets. You will be allowed to use a scientific calculator and you will sit this assessment paper at the end of Outcome 2.

The assessment for Outcome 3 will be based on a practical exercise lasting one hour followed by a report of 500 words minimum to be produced in your own time.

The assessment for Outcome 4 will be based a research exercise where a report of 500 words minimum will be produced in your own time.