Higher National Unit Specification

General information for centres

Unit title: Sequential Logic

Unit code: DG53 34

Unit purpose: The purpose of this Unit is to provide candidates with the necessary knowledge to understand the organisation of sequential logic devices and circuits, develop skills to design, simulate, build and test sequential logic circuits.

On completion of this Unit candidates should be able to:

1. Describe the characteristics of sequential logic circuits
2. Describe the operation of sequential logic devices
3. Design sequential logic circuits
4. Simulate, build and test sequential logic circuits

Credit value: 1 HN Credit at SCQF level 7: (8 SCQF credit points at SCQF level 7*)

**SCQF credit points are used to allocate credit to qualifications in the Scottish Credit and Qualifications Framework (SCQF). Each qualification in the Framework is allocated a number of SCQF credit points at an SCQF level. There are 12 SCQF levels, ranging from Access 1 to Doctorates.*

Recommended prior knowledge and skills: Candidates should possess a basic knowledge and understanding of combinational logic. This may be evidenced by the possession of the HN Unit Combinational Logic or NQ Units E9S3 11 Combinational Logic; E9SG 12 Sequential Logic; E9SB 12 Logic Families and Digital System Analysis or an appropriate equivalent.

Core skills: There may be opportunities to gather evidence towards Core Skills in this Unit, although there is no automatic certification of Core Skills or Core Skills components.

Context for delivery: This Unit was developed for the HNC/D Electronics awards. If this Unit is delivered as part of another group award, it is recommended that it should be taught and assessed within the subject area of the group award to which it contributes.

Higher National Unit Specification

General information for centres (cont)

Assessment: The assessment for Outcomes 1, 2 and the Shift Register Block Diagrams part of Outcome 3 is combined into one assessment paper. This paper should be taken by candidates at one single assessment event, lasting one hour. The assessment paper should be composed of a suitable balance of short answer, restricted response and written graphical exercises as specified for each Outcome. Assessment should be conducted under controlled, supervised conditions.

The design part of Outcome 3 should be carried out under closed book conditions followed by the Simulation, Build and Test Assessment for Outcome 4 carried out as an Assignment. The design – simulate - build and test should be done within 3 hours. It should be noted that candidates must achieve all the minimum evidence specified for each Outcome in order to pass the Unit.

Higher National Unit specification: statement of standards

Unit title: Sequential Logic

Unit code: DG53 34

The sections of the Unit stating the Outcomes, knowledge and/or skills and evidence requirements are mandatory.

Where evidence for Outcomes is assessed on a sample basis, the whole of the content listed in the knowledge and/or skills section must be taught and available for assessment. Candidates should not know in advance the items on which they will be assessed and different items should be sampled on each assessment occasion.

Outcome 1

Describe the characteristics of sequential logic circuits.

Knowledge and/or skills

- Difference between sequential and combinational circuits
- General block diagram of a sequential machine
- Difference between synchronous and asynchronous operations

Evidence requirements

A candidate's satisfactory performance in this Outcome can be evidenced by response to each of the three knowledge and /or skills elements as follows:

- Difference between combinational and sequential circuits

  Combinational circuit having no memory, same changes at inputs always produce same outputs, order that signals are applied at inputs is *not* important.
  Sequential circuit has memory, same changes at inputs can produce different output, order that signals are applied at inputs *is* important.

- General block diagram of a sequential machine

  Draw and label a block diagram for the general model of a sequential machine, indicate primary and secondary inputs, combinational logic network comprising logic gates, sequential logic network comprising bistables, feedback path and outputs. Describes the nature of each labelled element of the block diagram.

- Difference between synchronous and asynchronous operations

  Describe synchronous operation as clock driven, changes at outputs occurring in synchronisation with the circuit clock. Speed of operation is limited by frequency of the circuit clock.

Higher National Unit specification: statement of standards (cont)

Unit title: Sequential Logic

Describe asynchronous operation as having changes at outputs not synchronised with a circuit clock. Speed of operation determined by longest path through the circuit, due to propagation delays through individual devices.

Evidence should be gathered through assessment undertaken in controlled, supervised conditions. Assessment should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used for candidate evidence should take the form of a written and graphical exercises.

Outcome 2

Describe the operation of sequential logic devices

Knowledge and/or skills

- Cross-coupled latch using NAND or NOR gates
- SR, JK and D type bistables.
- Circuit symbols and state table for each bistable
- Function of synchronous and asynchronous inputs
- Edge triggered bistables
- Timing diagrams

Evidence requirements

A candidate's satisfactory performance in this Outcome can be evidenced by responses to each of the knowledge and/or skills elements as follows:

- Cross-coupled latch using NAND or NOR gates

  Draws cross-coupled NAND or NOR gates, identifies cross-coupled connection and feedback provides the memory property of a sequential device. Relates the circuit configuration to the sequential circuit model identifying primary inputs, secondary inputs, feedback and outputs. Determines the three operating modes of the circuit in terms of the Set and Reset input terminals, true and false Q output terminals. Action Table for circuit operation. States the effects of S-R inputs on Q outputs. Notes that in this form cross-coupled gates are operating asynchronously.

- SR, JK and D type bistables

  Identify modes of operation for SR, JK and D type bistable devices

Higher National Unit specification: statement of standards (cont)

Unit title: Sequential Logic

- Circuit symbols and state table for each bistable

  Draw and recognise circuit symbols and action tables for SR, JK and D type bistables.

- Function of synchronous and asynchronous inputs

  Function of synchronous and asynchronous inputs, incorporate into State/Action Table and Circuit Symbol for each bistable

- Clocked bistables

  Identify the phase of the clock that bistables are sensitive to, including rising and falling edges, low and high level

- Timing diagrams

  Interprets Waveform Timing Diagrams for SR, JK and D type bistables, including starting conditions and traces for synchronous and asynchronous inputs and outputs

Evidence should be gathered through assessment undertaken in controlled, supervised conditions and an assignment exercise to be submitted by the candidate. Assessment under controlled conditions should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment.

Assessment guidelines

Questions used for candidate evidence should take the form of a written and graphical exercise based on a Cross Coupled Latch and a Clocked Bistable sampling four responses from the six knowledge and/or skills elements.

Outcome 3

Design sequential logic circuits.

Knowledge and/or skills

- Design sequential circuits using bistables
- Asynchronous and synchronous counters
- State transition diagrams
- Counter MOD number
- Design of synchronous counters
- Use of Karnaugh maps and transition tables in counter design
- Design and implement sequence generators and detectors
- Shift registers: SISO, SIPO, PIPO, PISO, Universal
- Block Diagrams for serial and parallel shift registers

Higher National Unit specification: statement of standards (cont)

Unit title: Sequential Logic

Evidence requirements

A candidate's satisfactory performance in this Outcome can be evidenced by response to the following sample from the knowledge and /or skills elements:

- Design a synchronous sequential circuit for a sequence generator or a sequence detector using bistables and appropriate sequential logic techniques
- Produce a block diagram and a description of the operation of one of the five types of shift register listed

Evidence should be gathered by assessment undertaken in controlled, supervised conditions. Assessment under controlled conditions should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment other than device data sheets provided by the centre.

Assessment guidelines

The design exercise should consist of the design of a sequence generator or sequence detector. This design should be done as the first stage in a design, simulate, build and test assignment (see Outcome 4 for the simulate, build and test stages). Candidates should have access to appropriate data sheets. A question requiring the production of a block diagram for one type of shift register and the explanation of its operation should be included in the one hour assessment for Outcomes 1 and 2.

Outcome 4

Simulate, build and test sequential logic circuits.

Knowledge and/or skills

- Use logic tutor boards to verify state table for bistables
- Use software to simulate bistable based synchronous sequence generator or detector
- Build and test synchronous sequence generator or detector
- Use appropriate tools and techniques for circuit fault finding

Evidence requirements

A candidate's satisfactory requirement of this Outcome can be evidenced by response to the following sample of the knowledge and /or skills elements:

- Use software to simulate designs to be built and tested below
- Build and test synchronous sequence: generators or detectors

Logic tutors or similar are used to construct bistable based: synchronous sequence generators/counters from given output specification or synchronous sequence detectors from bit pattern specification

- Use appropriate tools and techniques for circuit fault finding

Evidence for the simulation should be gathered through assessment undertaken in controlled, supervised conditions and an assignment exercise to be submitted by the candidate. The build and test given as an assignment exercise is to be submitted by the candidate. Assessment under controlled conditions should be conducted under closed book conditions and as such candidates should not be allowed to bring any textbooks, handouts or notes to the assessment other than device data sheets and design specifications provided by the centre.

Assessment guidelines

The assessment for this Outcome should consist of an assignment involving the computer simulation and construction of the sequence generator or sequence detector design in Outcome 3. An observational checklist should be used to record candidate progress.

Administrative Information

Unit code: DG53 34

Unit title: Sequential Logic

Superclass category: XL

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Source: SQA

Higher National Unit specification: support notes

Unit title: Sequential Logic

This part of the Unit specification is offered as guidance. The support notes are not mandatory.

While the exact time allocated to this Unit is at the discretion of the centre, the notional design length is 40 hours.

Guidance on the content and context for this Unit

Candidates should be made aware during the unit introduction of the wide application for sequential logic techniques in society today. Sequential logic is found in the Personal Computer and associated peripheral devices, mobile phone technology, MP3 Players, Mini Discs, satellite communication and is the major technology behind the Internet. Sequential logic can be found to be controlling and directing information in routers, switches and hubs. It should be emphasised that although the subject of sequential logic is a specialist area it is based on well-understood combinational logic and as such candidates have already been studying sequential logic techniques in earlier courses such as NQ and HN Units Combinational Logic.

Outcome 1: The general block diagram of a sequential circuit introduced in Outcome 1 can be used to clarify the connection between the candidates existing knowledge and the new sequential techniques to be learned in this Unit. All of the knowledge and techniques learned to design combinational logic circuits - logic expressions, truth tables and Karnaugh mapping techniques will be used throughout this Unit. The Sequential circuit Model described by the general block diagram should also be used throughout the Unit to place the circuits being discussed in context. Gates, Truth Tables and combinational logic techniques being used to design the Combinational Logic Network whereas Bistables, Action Tables and knowledge of specific sequential logic techniques are used to design the Sequential Logic Network. After studying Outcome 1 the candidate should be able to:

- Describe the difference between combinational and sequential circuits
- Draw and label the General block diagram of sequential machine
- Describe the difference between asynchronous and synchronous operations

Outcome 2: The cross-coupled gates forming the latch of Outcome 2 can again be viewed and compared against the Sequential Logic General Block Diagram. The use of the SR Latch for switch contact de-bounce could be used as a common practical application of this configuration. Some time should be spent familiarising candidates with the modes of operation of the SR latch and other bistables, before moving on to clocked bistables it should be emphasised that the operating modes are the same — it is just *when* the device is active that is different - depending on the state of asynchronous inputs and the low, rising, high and falling states of the synchronous clock input. Sufficient time should be given to practical activities in this Outcome to allow candidates to further develop their construction skills and device understanding before moving on to formative assessment.

Higher National Unit specification: support notes (cont)

Unit title: Sequential Logic

After studying Outcome 2 the candidate should be able to:

Relating to an SR Latch
- Draw a Latch based on Cross Coupled gates
- Compare Latch to Sequential Model
- Draw Action Table
- State the effect of SR inputs on the Q output

Relating to a specified Clocked Bistables
- Draw the Circuit symbol
- Draw the Action Table
- Identify the sensitive phase of the clock
- Describe the function of Synchronous inputs
- Describe the function of Asynchronous inputs
- Interpret Waveform Timing Diagrams

Outcome 3: In Outcome 3 the ripple counter is used as an example of an asynchronous sequential logic circuit. This provides an opportunity to discuss the accumulative propagation delay limitations of multi-stage ripple counters and reset noise. The Unit is not intended to cover the asynchronous design process in detail, the main emphasis is in the design of bistable based synchronous sequential circuits using appropriate techniques such as the state transition diagram, state transition table and the use of Karnaugh maps for simplification of next state logic equations. Other design techniques can be used in a similar consistent manner. The end product should be correct logic circuit diagrams detailed in the knowledge and/or skills evidence requirement sections.

After studying Outcome 3 the candidate should be able to:

- Produce a design based on bistables for a Sequence Generator or Sequence Detector from specified bit pattern
- Draw a block diagram for a specified shift register configuration and describe an element of its operation.

Outcome 4: Outcome 4 concentrates on simulation, build and testing of devices, synchronous counters, sequence generators and detectors specified in Outcomes 2 and 3. As there are no MSI devices used early versions of Electronics Workbench found in most colleges and provided free through software schemes should be adequate to simulate all designs, other low cost simulation programmes should be sufficient. Logic tutors should be used throughout to implement the circuits both formatively and summatively, candidates should be encouraged to develop techniques to keep track of wiring during construction and organise the testing of circuits by drawing up test tables to record circuit operation. Candidates should also be allowed to develop their testing and fault finding skills further using state transition diagrams to track the operation of completed designs and encouraged to correct any circuit faults encountered.

Higher National Unit specification: support notes (cont)

Unit title: Sequential Logic

After studying Outcome 4 the candidate should be able to:

- Build and Test Clocked Bistables from Outcome 2
- Simulate Sequence Generator or Sequence Detector designed in Outcome 3
- Build and Test Sequence Generator or Sequence Detector designed in Outcome 3

Guidance on the delivery and assessment of this Unit

Timing of this Unit would normally be in the first year of an HNC/HND immediately after completion of the HN Unit Combinational Logic. On completion of Sequential logic candidates can progress on to the HN Unit Programmable Logic Devices or MSI Devices this progression fits in with a 2 semesters or 3-term first and second year HND.

Assessment for Outcomes 3 and 4 should follow the recognised order of design, simulate build and test. A holistic approach should be adopted to emphasise the recursive nature of the design – simulate – build – test cycle.

The instruments of assessment for Outcome 1 should be restricted to a written/graphical exercise. A written graphical exercise testing the Knowledge element should also be used for Outcome 2; assignment exercises and computer simulation packages providing candidates with practical experience of using bistables will help understanding and knowledge retention.

Assessment for Outcome 3 has two elements, the first takes the form of a short answer/graphical test covering the operation of and block diagrams for listed shift registers carried out under closed book examination conditions. The second element is a design exercise, this should be done under controlled conditions with access only to relevant data sheets provided. Again practical assignment exercises and computer simulation packages can be used to develop and enhance candidate understanding of the knowledge and/or skills elements, the design exercise for Outcome 3 will be simulated, built and tested as the assessment for Outcome 4.

It is recommended that Outcomes 1 and 2 and the shift register operation/block diagram element of Outcome 3 be assessed using a single paper of 1 hour duration at the end of the Unit.

The design element of Outcome 3 should be carried out under closed book examination conditions with access to appropriate data sheets, the design should be completed within 1 hour.

The assessment for Outcome 4 should be carried out in a less formal and relaxed setting to encourage candidates to experiment and share ideas, however care should be taken to ensure that evidence is candidates own work and observational checklists should be used to record candidates progress through practical assignments and simulation exercises where they contribute towards summative assessment for Outcome 4.

Higher National Unit specification: support notes (cont)

Unit title: Sequential Logic

The complete design, simulate, build and test assessment should take a total of three hours.

Open learning

This Unit could be delivered by distance learning or flexibly, however the centre would have to provide access to a logic tutor and suitable software to support the considerable amount of practical activity required for developing the skills to meet the assessment requirements of Outcome 4. Centres would also take steps to ensure that their quality assurance systems can be extended to cover the open learning mode of delivery.

For further advice on this aspect of delivery see the SQA publication *Assessment and Quality Assurance for Open and Distance Learning* (Feb. 2001 code A1030).

Special needs

This Unit specification is intended to ensure that there are no artificial barriers to learning or assessment. Special needs of individual candidates should be taken into account when planning learning experiences, selecting assessment instruments or considering special alternative Outcomes for Units. For information on these, please refer to the SQA document *Guidance on Special Assessment Arrangements* (SQA, 2001).

General information for candidates

Unit title: Sequential Logic

Much of the developments seen today in modern technology are down to the techniques you will study in this Unit - computers, internet technology - switches hubs and routers, CD and DVD technology, Mini Disks, MP3 players, Electronic Musical Instruments, MIDI, MP3 players, mobile phones, satellite communications, CAD/CAM systems — the list goes on and on.

This Unit has been designed to provide you with the knowledge and skills that will enable you to understand the important techniques of Sequential Logic. You will learn how Sequential Logic Circuits are organised, how they are different from Combinational Logic Circuits and also how they are constructed using a mixture of gates and bistables.

When you studied Combinational logic you learned about the basic building block of a combinational logic circuit - the gate; in this Unit you will learn about the basic building block of a Sequential Logic circuit - the Bistable.

You will investigate the operation of the most common bistables and how they can be connected to form Sequential Logic Circuits.

You will learn how to design the two major classes of sequential circuit - the Sequence Generator and the Sequence Detector, these circuits are at the heart of all of the technologies mentioned above.

In modern electronic design computers are used to simulate designs before going to the expense of production, in this Unit you will learn how to simulate your designs on computer.

This Unit will also allow you to develop practical skills that will enable you to successfully build and test the designs you have created.

The precise form the assessment will take will depend on the Centre where you are taking the Unit. You will be required to undertake both written graphical, computer simulation and practical assessments.

The following is a guide to what you should be able to do after completing each Outcome:

Outcome 1

- Describe the difference between combinational and sequential circuits
- Draw and label the general block diagram of sequential machine
- Describe the difference between synchronous and asynchronous operations

General information for candidates (cont)

Unit title: Sequential Logic

Outcome 2

Relating to the SR Latch

- Draw Latch circuits based on Cross Coupled NAND/NOR gates
- Compare Latch circuits to Sequential Model
- Draw SR Latch Action Tables

Relating to specified Clocked Bistables

- Draw the circuit symbols
- Draw the Action Tables
- Identify the sensitive phase of clocks
- Describe the function of Synchronous Inputs
- Describe the function of Asynchronous inputs
- Interpret Waveform Timing Diagrams

Outcome 3

- Produce a Design for Sequence Generators/Sequence Detectors from specified bit patterns
- Draw circuit diagrams for specified shift register configurations.

Outcome 4

- Construct and Test Cross coupled NAND/NOR gates
- Build and test Clocked Bistables from Outcome 2
- Simulate Sequence Generators/Sequence Detectors designed in Outcome 3
- Build and Test Sequence Generators/Sequence Detectors designed in Outcome 3

Written graphical assessments will take place under controlled, supervised conditions. It will be carried out under closed book conditions in which you will not be allowed to take notes, handouts, textbooks etc into the assessment, you will however be allowed to use the data sheets provided by your centre. Please ask your lecturer for the details on how you will be assessed and the datasheets you will be given.

You will be required to carry out computer simulation of your designs before building and testing them.

Your practical skills will be assessed by means of assignments in which you will be required to satisfactorily complete a series of tasks that will enable you to build and test your sequential logic designs. Assignments must be handed in by the date specified by your lecturer.