Course report 2019

Subject	Practical Electronics
Level	National 5

This report provides information on candidates' performance. Teachers, lecturers and assessors may find it useful when preparing candidates for future assessment. The report is intended to be constructive and informative and to promote better understanding. It would be helpful to read this report in conjunction with the published assessment documents and marking instructions.

The statistics used in this report have been compiled before the completion of any post-results services.

Section 1: comments on the assessment

Question paper

The question paper performed as expected with feedback from both the marking team and teachers and lecturers indicating that it was fair both in terms of course coverage and overall level of challenge. Analysis of the question paper results showed that all questions were answered correctly by the majority of candidates, and that there was a spread of performance across the range of available marks.

Practical activity

This practical activity encompasses a wide range of activities that allows for differentiation between candidates. These range from the practical elements such as soldering, wiring and assembly skills, working safely and independently through to the more demanding tasks such as circuit design and simulation, circuit layout plans, circuit testing and evaluation.

Section 2: comments on candidate performance

Areas that candidates performed well in

Question paper

In the following questions, candidates performed well:

Question 1 (a)	The majority of candidates could name, identify or describe the function of selected components.
Question 1 (b) (i)	The majority of candidates could determine the value of the resistor from its colour bands.
Question 1 (b) (ii)	The majority of candidates could determine the minimum and maximum value of the resistor.
Question 3 (a) (i)	Most candidates could calculate the series resistance.
Question 3 (a) (ii)	Most candidates could apply Ohm's law to calculate current.
Question 3 (b)	Most candidates could calculate the parallel resistance.
Question 4 (a)	Most candidates could draw the symbol for a NAND gate.
Question 4 (c)	The majority of candidates could complete a truth table for a combination of three logic gates.
Question 5 (a)	The majority of candidates could identify the errors in the set-up of the multimeter.
Question 8 (a)	The majority of candidates could complete a pre-power up checklist.
Question 8 (b)	The majority of candidates could identify the errors in the simulation.
Question 9	The majority of candidates could score at least 3 marks in the production of a block diagram.

It was noted by the marking team that more candidates completed the 'system/block diagram' and 'layout diagram' questions with greater success than in 2018.

Practical activity

Overall, candidates performed well in the more practical aspects of the task. These consist of circuit construction, wiring and assembly, as well as circuit simulation. This accounts for 51 marks of the available 70. Candidates should be suitably experienced in these elements before assessment. It is essential that candidates have access to a suitable range of properly-maintained tools and equipment, in order to complete these tasks.

Areas that candidates found demanding

Question paper

Question 2 (a)	The majority of candidates were unable to explain how an electromagnet works with the required level of technical accuracy.
Question 2 (b) (i)	The majority of candidates were unable to identify the wiring technique.

Question 2 (b) (ii)	The majority of candidates could not explain why the wiring technique was used.
Question 3 (a) (iii)	Many candidates could not calculate the power dissipated.
Question 4 (b)	Many candidates were unable to name the logic gate that produces the truth table shown.
Question 5 (b)	Many candidates could not fully explain the correct procedure to measure an unknown resistance using a multimeter. Some responses lacked the clarity required to be awarded more marks.
Question 6 (a)	In the CRO frequency calculation, some candidates found converting milliseconds to seconds challenging.
Question 6 (b)	A significantly high number of candidates could not identify an analogue waveform from a CRO screen.
Question 7 (a)	Many candidates failed to recognise that the reference voltage Vx was the voltage across the 4K resistor. Many candidates gave no response.
Question 7 (b)	Candidates found this to be the most challenging question with many candidates giving no response.
Question 7 (c)	Candidates found this to be a challenging question with a significant number of candidates making no attempt to answer the question. Of those who did, many struggled to provide an adequate description, with responses often lacking the clarity and precision required to be awarded more marks.
Question 10	More candidates attempted the 'layout diagram' question compared to last year. Of those who did, many were able to gain at least some marks. However it was apparent that the inclusion of the pnp transistor presented difficulties for a few candidates.

A very small number of candidates had either not prepared for, or did not appreciate the depth of understanding and application of knowledge required for, the question paper.

Where candidates were asked to describe or explain, answers were often too short or lacked sufficient detail or technical accuracy to gain marks. Candidates should pay attention to the command word used in each question and answer accordingly in order to be awarded marks.

Practical activity

Candidates found the initial analysis of the given problem, which is worth 7 marks, challenging. Candidates analysing the given task correctly with accurately-labelled diagrams can achieve the maximum 7 marks, whereas others will be guided and marked accordingly in order to proceed with the rest of the assignment.
The final 12 marks can be demanding for candidates. They consist of 7 marks for testing the solution and 5 marks for reporting and evaluation. Key to gaining these marks are the candidate's ability to keep clear and accurate project logbooks detailing key stages in the assignment, and the ability to evaluate the completed circuit test results against the simulation test results and the given task specification.

Section 3: preparing candidates for future assessment

Question paper

Candidates answering questions which require either restricted or extended-responses should be wary of over-elaboration. Some candidates could identify errors in simulations but could not express themselves with the required degree of clarity or precision to gain the mark.

Centres should ensure that candidates can describe, in a succinct and precise way, how to use the various instruments described in the course specification. In terms of applying relationships, candidates found calculating the reference voltage of a LM741 comparator very challenging and may need more practice in voltage division in general.

Candidates need to be able to explain how a comparator and a transistor controlled circuit works. Many candidates did not fully understand the relationship between voltage and resistance in a series circuit. Most candidates are now aware that when they are asked to draw circuit diagrams, they should ensure that there is a node on the end of the V+ and 0V lines.

Candidates need to be aware of both types of bi-polar transistors (pnp as well as npn) and how these are positioned in simulations and circuit diagrams.

Centres should be aware that most typical ‘A type’ questions are those which require the candidate to take information from one conceptual format and present it in another, for example, in block diagrams or when transferring a layout diagram to a circuit diagram (or vice versa).

Practical activity

Teachers and lecturers should ensure that candidates are well prepared for the less demanding tasks such as circuit construction, wiring and assembly, as well as circuit simulation.

For example, good circuit simulation should include a range of circuit performance results. This will assist candidates when testing the actual solution that they build in order to compare actual test results with the simulation results. This will also assist candidates in achieving marks in the construction section for the inclusion of test points in their circuits, and assist with the reporting section.

Centres should give candidates access to a suitable range of properly-maintained tools and equipment. Candidates will also need to gain experience of using these tools and equipment as well as the simulation software.

In addition, candidates need to be encouraged to give clear, legible, fully annotated and accurate drawings and circuits at all stages in order to achieve maximum marks at the practical stages. All components should be properly labelled on circuits and in diagrams. Candidates should be encouraged to see each major stage of the assignment as a milestone that should be clearly documented and understood by others.

The more demanding tasks of testing and reporting are dependent upon candidates including a range of circuit performance results from their simulation. This will assist them when testing the actual solution built in order to compare actual test results with the simulation test results and the given task specification.

Grade boundary and statistical information:

Statistical information: update on courses

Number of resulted entries in 2018	179

Number of resulted entries in 2019	209

Statistical information: performance of candidates

Distribution of course awards including grade boundaries

Distribution of course awards	Percentage	Cumulative %	Number of candidates	Lowest mark
Maximum mark				
A	39.2%	39.2%	82	70
B	25.4%	64.6%	53	60
C	22.0%	86.6%	46	50
D	9.1%	95.7%	19	40
No award	4.3%	-	9	-

General commentary on grade boundaries

SQA's main aim is to be fair to candidates across all subjects and all levels and maintain comparable standards across the years, even as arrangements evolve and change.

SQA aims to set examinations and create marking instructions that allow:

- a competent candidate to score a minimum of 50% of the available marks (the notional C boundary)
- a well-prepared, very competent candidate to score at least 70% of the available marks (the notional A boundary)

It is very challenging to get the standard on target every year, in every subject at every level.

Therefore, SQA holds a grade boundary meeting every year for each subject at each level to bring together all the information available (statistical and judgemental). The principal assessor and SQA qualifications manager meet with the relevant SQA head of service and statistician to discuss the evidence and make decisions. Members of the SQA management team chair these meetings. SQA can adjust the grade boundaries as a result of the meetings. This allows the pass rate to be unaffected in circumstances where there is evidence that the question paper has been more, or less, challenging than usual.

- The grade boundaries can be adjusted downwards if there is evidence that the question paper is more challenging than usual.
- The grade boundaries can be adjusted upwards if there is evidence that the exam is less challenging than usual.
- Where standards are comparable to previous years, similar grade boundaries are maintained.

Grade boundaries from question papers in the same subject at the same level tend to be marginally different year to year. This is because the particular questions, and the mix of questions, are different. This is also the case for question papers set by centres. If SQA alters a boundary, this does not mean that centres should necessarily alter their boundary in the question papers that they set themselves.