Course Report 2017: Internally Assessed Course Component

Subject	Practical Electronics
Level	National 5

The statistics used in this report have been compiled before the completion of any Post Results Services.

This report provides information on the performance of candidates which it is hoped will be useful to teachers, lecturers and assessors in their preparation of candidates for future assessment. It is intended to be constructive and informative and to promote better understanding. It would be helpful to read this report in conjunction with the published assessment documents and marking instructions.

Section 1: Comments on the assessment

The practical aspects of the task are generally achieved well, but there is a lack of detailed information at the design, testing and reporting stages of the task. It is anticipated that the revised marking scheme for next session will result in more detail from candidates with regard to the design, testing and reporting stages — this will encourage candidates to be more analytical, as these stages are just as important as the build stage of the task.

The range of tasks provided performed as expected this session with a wide spread of results achieved by candidates.

The following observations were noted with regard to assessment approaches from this round of verification visits:

- Logbooks and photographic evidence were kept by each candidate, reflecting progress throughout the activity.
- Suitable guidance was given and noted by assessors, making tracking of candidate progress visible.
- Adequate and well maintained laboratory resources were available for candidates to complete the activity successfully.
- A good standard of soldering and electronics construction techniques was demonstrated throughout.
- Candidates would benefit from being more methodical with regards to testing strategies and implementation from pre-power up checks, identifying critical testing points through to full function testing, but this can be difficult at this level.

Candidates found the evaluation difficult. It is recommended that candidates keep a record of faults found and fixed, and discuss these in the evaluation.

Candidates should be assessed on the extent to which the stripboard plans match the physical circuit. To aid with this, candidates should use ‘physical’ symbols showing the exact dimensions and holes occupied by each component — not circuit symbols. Additionally, each component in the plan should be given a unique component ID which is consistent with the candidate’s simulation and component list. All I/Os should be clearly labelled, along with a clear label of which board is input, process and output.

Candidates should be assessed on their ability to route components. It is good practice not to route wires or resistors over the top of ICs or protection diodes over the top of relays.

There was some evidence of looming, but there were a lot of hard-wired or loose wires.

Candidates should receive greater outline guidance when discussing the initial brief with their assessor. It is advisable to raise candidates’ awareness of issues arising from their choice of solutions that will negatively impact on their assignment later in the process. It is essential that the assessor fully appreciates the level of detail required at this early stage of the assignment, as this has consequences for assessment later in the assignment.

Candidates’ attention can be drawn to previous areas of work which presented similar challenges — but leave it to them to transfer previously-accumulated knowledge and skills should they chose to do so. One particular area which falls into this category is 3d wiring and

assembly (loom quality). The assessor should make ongoing judgments as candidates progress to completion, and interact and mark accordingly.

Candidates should be assessed on their ability to form and place components. To aid success in this area, the centre could encourage soldering in order of lowest to highest profile, thus reducing the tendency of the component to have space to fall out during soldering. The assessor should judge the extent to which a candidate has checked the soldering of components like DIL sockets as they construct the circuit.

Candidates should be assessed on the use of cable markers, crimp/block connections, shrink wrap/spiral wrap/cable ties along with documentation, for example a table, detailing the marker ID with a start and end-point.

Section 2: Comments on candidate performance

Areas in which candidates performed well

The construction part of the task is generally achieved well due to candidates gaining practical 'hands on' experience in constructing electronic circuits. To achieve this, centres require access to a suitable range of tools and equipment that is sufficient for the number of candidates. Tools and equipment must be properly maintained — candidates can easily become frustrated if these do not perform as expected.

In general, candidates were encouraged to be neat and methodical with regard to circuit layout and construction. A reasonably high standard of soldering and other construction skills was achieved.

Candidates also performed well using simulation software to ensure a working circuit, but greater emphasis could be placed on using the simulation software to also produce a testing plan for the circuit which can be used to check against actual test results achieved. Comparisons can then be made. This will aid the testing and reporting stages.

Areas which candidates found demanding

The design, planning, testing and eventual reporting stages are, in general, very demanding as candidates focus on the practical skills and not necessarily the documentation stages. To assist candidates with these demanding stages, it may be that they need additional guidance/documentation on the standards required of the documentation. The purpose of any additional documentation should be to encourage and help candidates through these demanding stages.

Section 3: Advice for the preparation of future candidates

Centres should endeavour to encourage candidates towards more documented evidence with regard to the four major milestones in the task, ie design, construction, testing and reporting. Candidates will naturally wish to build the circuit and get it working, but they should be steered towards creating comprehensive documentation at National 5 level as they proceed through the task.

Grade Boundary and Statistical information

Statistical information: update on courses

Number of resulted entries in 2016	119

Number of resulted entries in 2017	210

Statistical information: Performance of candidates

Distribution of course awards including grade boundaries

Distribution of course awards	%	Cum. %	Number of candidates	Lowest mark
Maximum Mark -				
A	37.1%	37.1%	78	56
B	23.3%	60.5%	49	48
C	17.1%	77.6%	36	40
D	6.7%	84.3%	14	36
No award	15.7%	-	33	-

General commentary on grade boundaries

- While SQA aims to set examinations and create marking instructions which will allow a competent candidate to score a minimum of 50% of the available marks (the notional C boundary) and a well prepared, very competent candidate to score at least 70% of the available marks (the notional A boundary), it is very challenging to get the standard on target every year, in every subject at every level.

- Each year, SQA therefore holds a grade boundary meeting for each subject at each level where it brings together all the information available (statistical and judgemental). The Principal Assessor and SQA Qualifications Manager meet with the relevant SQA Business Manager and Statistician to discuss the evidence and make decisions. The meetings are chaired by members of the management team at SQA.

- The grade boundaries can be adjusted downwards if there is evidence that the exam is more challenging than usual, allowing the pass rate to be unaffected by this circumstance.

- The grade boundaries can be adjusted upwards if there is evidence that the exam is less challenging than usual, allowing the pass rate to be unaffected by this circumstance.

- Where standards are comparable to previous years, similar grade boundaries are maintained.

- An exam paper at a particular level in a subject in one year tends to have a marginally different set of grade boundaries from exam papers in that subject at that level in other years. This is because the particular questions, and the mix of questions, are different. This is also the case for exams set in centres. If SQA has already altered a boundary in a particular year in, say, Higher Chemistry, this does not mean that centres should necessarily alter boundaries in their prelim exam in Higher Chemistry. The two are not that closely related, as they do not contain identical questions.

- SQA's main aim is to be fair to candidates across all subjects and all levels and maintain comparable standards across the years, even as arrangements evolve and change.