NQ Verification 2016–17
Key Messages Round 2

01

Section 1: Verification group information

Verification group name:	**Practical Electronics**
Verification event/visiting information	**Visiting**
Date published:	**June 2017**

National Courses/Units verified:

Unit code C760 level National 5 Unit title Practical Electronics IACCA

02

Section 2: Comments on assessment

Assessment approaches

The following observations were noted with regard to assessment approaches from this round of verification visits:

1

Logbooks and photographic evidence was kept by each candidate, reflecting progress throughout the activity. Suitable guidance was given and noted by assessors, making tracking of candidate progress visible. Adequate and well maintained laboratory resources were available for candidates to complete the activity successfully. A good standard of soldering and electronics construction techniques was demonstrated throughout. Candidates would benefit from being more methodical with regards to testing strategies and implementation from pre-power-up checks, identifying critical testing points through to full function testing, but this can be difficult at this level.

2

Candidates found the evaluation difficult. It is recommended that a record of faults found and fixed is kept by candidates and discussed in the evaluation.

Candidates should be assessed on the extent to which the stripboard plans match the physical circuit. To aid with this, candidates should use ‘physical’ symbols showing the exact dimensions and holes occupied by each component, and not circuit symbols. Additionally, each component in the plan should be given a unique component ID that is consistent with the candidate’s simulation and component list. All I/Os should be clearly labelled, along with a clear label of which board is input, process and output.

Candidates should be assessed on their ability to route components. It is good practice not to route wires or resistors over the top of IC’s or protection diodes over the top of relays.

There was some evidence of looming, but there were a lot of hard-wired or loose wires. Candidates should be assessed on the use of cable markers, crimp/block connections, shrink wrap/spiral wrap/cable ties along with documentation, for example a table, detailing the marker ID with a start and end-point.

3

Candidates should receive greater outline guidance when discussing the initial brief with their assessor. It is advisable to raise candidate awareness of issues arising from their choice of solutions that will negatively impact on their assignment later in the process. It is essential that the assessor fully appreciates the level of detail required at this early stage of the assignment, as this has further consequences for assessment later in the assignment.

4

Candidates’ attention can be drawn to previous areas of work which presented similar challenges, but leave it to them to transfer previously accumulated knowledge and skills should they chose to do so. One particular area that falls into this category is 3D wiring and assembly (loom quality). The assessor should make ongoing judgments as candidates progress to completion and interact and mark accordingly.

5

Candidates should be assessed on the extent to which the stripboard plans match the physical circuit. To aid with this, candidates should use ‘physical’ symbols showing the exact dimensions and holes occupied by each component, and not circuit symbols. Additionally, each component in the plan should be given a unique component ID which is consistent with the candidate’s simulation and component list. All I/Os should be clearly labelled along with a clear label of which board is input, process and output.

Candidates should be assessed on their ability to form and place components. To aid success in this area, the centre could encourage soldering in order of lowest to highest profile, thus reducing the tendency of the component to have space to

fall out during soldering. The assessor should judge the extent to which candidates have checked the soldering of components like DIL sockets as they construct the circuit.

6

Candidates should be assessed on the use of cable markers, crimp/block connections, shrink wrap/spiral wrap/cable ties along with documentation, for example a table, detailing the marker ID with a start and end-point.

Assessment judgement

The following observations were noted with regard to assessment judgement from this round of verification visits:

1

There is a team of three involved in the marking process with clear communications across the team. Spreadsheets are created for each candidate indicating progress throughout the activity, with good use of photographs and logbooks showing interim progress as well as the final constructed circuits. Clear and constructive comments from assessors on the mark allocations will make the process of internal and external verification more robust.

2

The centre should reference the descriptors more accurately when awarding marks in each section of the assignment.

3

The assessor experienced difficulty in marking candidates in two sections of the marking scheme, namely section 1 and 3b to the appropriate standard. This was due to a lack of experience in this area.

4

The category 3D wiring and assembly component presented some challenges when making judgements, but this only affected a small number of candidates who had chosen rather unusual electronic solutions to the assignment specification. The centre provided some commentary in the assessment record against the marks awarded. It was useful to have a brief explanation as to why the selected marks had been awarded.

5

Although the assessor commented on the standard of the candidate’s work, there was little written evidence on how independently each candidate worked or the level of guidance given by the centre. This information could be recorded in the candidate’s log or added to the comments section of the overall mark sheet.

Candidates should be assessed on the extent to which they fully utilise simulation tools. Schematics with unconnected wires as inputs/outputs cannot possibly

simulate functionality. The centre should judge the use of logic level indicators when demonstrating functionality of discrete input, process and output sub systems.

6

Candidates should be assessed on the extent to which the stripboard plans match the physical circuit. To aid with this, candidates should use ‘physical’ symbols showing the exact dimensions and holes occupied by each component and not circuit symbols. Additionally, each component in the plan should be given a unique component ID which is consistent with the candidate’s simulation and component list. All I/Os should be clearly labelled along with a clear label of which board is input, process and output. There was little evidence of looming and many insecure wires.

Candidates should be assessed on the use of cable markers, crimp/block connections, shrink wrap/spiral wrap/cable ties along with documentation, for example a table, detailing the marker ID with a start and end- point.

03 Section 3: General comments

The design, planning, testing and eventual reporting stages are, in general very demanding as candidates focus on the practical skills and not necessarily the documentation stages. To assist candidates with these demanding stages, it may be that additional guidance/documentation is required on the standards to be met for the documentation stages. The purpose of any additional documentation should be to encourage and help candidates through these demanding stages.

Centres should endeavour to encourage candidates towards more documented evidence with regard to the four major milestones in the task, ie design, construction, testing and reporting. Candidates will naturally wish to build the circuit and get it working, but should be steered towards creating comprehensive documentation at National 5 level as they proceed through the task.