NQ verification 2022–23 round 2

Qualification verification summary report

Section 1: verification group information

Verification group name:	**Practical Electronics**
Verification activity:	**Visit**
Date published:	**June 2023**

National Course verified

Unit code	Unit level	Unit title
C860 75	National 5	Practical Electronics: Practical activity

Section 2: comments on assessment

Assessment approaches

All centres used one of SQA's mandatory course assessment tasks for the practical activity. Centres selected from a bank of tasks that are all similar in complexity and provide sufficient opportunity for candidates to demonstrate different levels of performance, from analysis and design through to construction, testing, and final reporting.

Regardless of the task chosen or the experience of the assessor, candidates did well at certain stages and found other stages of the practical activity challenging. In all tasks, candidates found creating circuit layout diagrams, creating test plans and final circuit analysis challenging. The more practical, less reflective tasks (such as circuit simulation and construction) were performed reasonably well by candidates.

Of the 20 centres verified, 14 received an 'accepted' outcome with no recommendations and the other 6 received an 'accepted*' outcome with recommendations for their approach to assessment.

Assessment judgements

Overall, all centres made accurate and reliable judgements, with all 20 centres receiving an ‘accepted’ or ‘accepted*’ outcome for assessment judgements. Although there were some discrepancies with candidate marks, each was within tolerance, demonstrating a sound understanding of national standards.

Where a centre had an ‘accepted*’, this was usually due to inexperience in delivering the course. This was also true with the industrial aspects of electronics, such as clarity of layout diagrams and conventions used (colour coding of layout wires), interconnection techniques for circuit boards and test planning.

In some instances, deviations in marks were down to whether assessors gave candidates real time feedback or at the end of milestones. For example, candidates construct three circuits and, if assessors provide them with suitable feedback after constructing the first circuit, this gives candidates the opportunity to improve marks for the second and third circuits. If assessors only give feedback at the very end, then mistakes may be repeated and candidates drop 2 or 3 marks out of 31 marks for the construction element of the task. It is recommended that, as circuits are constructed, each board is checked for accuracy and that assessors give suitable feedback to ensure that candidates can improve marks for the remaining circuits.

Points to note regarding assessment approaches and assessment judgements

Analysis and design:

- It is good practice for schematic diagram to have directional arrows, however it is not a requirement of the course, so candidates can still gain full marks without them.
- In general, costing and component lists were not well done. For a detailed list of components, candidates should use a table that has a list of components, serial code, number of components, supplier, unit price and total price. To work out the total price of each type of component, candidates should investigate the price for a batch of components, rather than multiplying the unit price by the number of components.
- Candidates may benefit from compiling the components list from the simulation and, when they reach the construction stage, go back to the listing and add components (such as the 8-way and 14-way DIL sockets). If candidates adopt this approach, assessors should mark the component list at the end of the construction stage.
- The bill of materials should include an "item ID" (for example R1, R2, LED 1, IC1, TR1, BZ1). Candidates should carry the item ID through to the Yenka simulation, breadboard planning, stripboard (layout) planning and testing.

Designing and simulating a solution:

- In most instances, candidates who struggled to produce a stripboard layout were correctly provided with a fully annotated solution to use for circuit construction. This allowed candidates, without a fully working layout diagram, the opportunity to access all marks in the later construction stage.
- Yenka simulations were not always clearly sectioned off and labelled with input, process and output.

- Layout diagrams should include all interconnections and track cuts. Candidates should create them using the actual footprint of each component and not the simulation circuit symbol.
- It is good practice to plan and include test points in the layout diagram. Doing this should help candidates with the testing stage later.
- There was leniency when assessing 'Detailed component layout diagrams'. Some candidates had no track breaks, or the breaks were in the wrong place.

Constructing the solution:

- The standard of soldering observed was of an excellent standard, which is encouraging.
- The actual circuits constructed should replicate the layout diagrams to ensure consistency. However, it may be necessary to make changes, such as axial capacitors could become radial capacitors due to component ordering.
- The stripboard plans and physical circuit should match exactly.
- It is good practice not to solder an IC onto stripboard, as it may damage the components inside it. A dual-in-line holder should be soldered first.
- Candidates must use wiring conventions. They should only use red wire for power connections, both on the individual boards and in the loom, and black wire for ground connections. They can use any other colour of wire for signals. Centres must always have three colours of wire for candidates to use. If red wire and black wire are not available, the centre should document what two colours they are using, so candidates cannot use these two colours for any signal wiring. When candidates followed wiring conventions, this helped them during circuit construction and to identify faults during testing and repair.
- Centres can purchase professional circuit labelling kits to save candidates using marker pens to label stripboards.
- Candidates should be assessed on the use of colour coding or numbering of each wire, cable markers, crimp and block connections, and shrink wrap, spiral wrap and cable ties.
- Leads between circuit boards should be protected by using sleeving or some other form of protection, or spiral wrap rather than black heat shrink sleeving.
- Input, process and output boards should be easily disconnected from each other using either crimp connectors or terminal blocks in the wiring looms.
- For 'Neatness of sub-system layout', assess candidates on colour codes with the correction convention. For example, pin 14 should be connected to +Vs rail with a red wire, pin 7 should be connected to 0 V rail with a black wire.
- When assessing each sub-system, provide comments to justify marks awarded to candidates for ‘working safely’ and ‘working independently’ during construction.

Testing the solution:

- Encourage candidates to present three test plans — pre-testing each sub-system, power testing each sub-system, and power testing the three sub-systems connected together.
- Candidates benefit from access to consumables that allow the insertion of fixed test points at circuit nodes, and that tie into their test plans. This helps them when taking measurements during testing and making subsequent repairs.
- It is good practice to put pre-power up checks in a table, instead of written as paragraphs.

- Candidates did not always use a logic probe for testing, instead some used a multimeter set on voltage and tried to record values. This made taking tests considerably more difficult, as the voltage shown on a multimeter is not easily assimilated to corresponding logic levels.

Reporting on the solution:

- This stage of the practical activity was assessed reliably and consistently.
- Candidates would benefit from recording test results using bullet points or in a table, instead of writing long paragraphs.

Section 3: general comments

The practical activity has a good balance of hands-on elements, as well as more demanding tasks such as circuit layout diagrams, testing and evaluation.

Experienced assessors were able to guide candidates to perform better, however, there is a wealth of support for all assessors to tap into if they wish. For example, the marking instructions (supported by Understanding Standards materials) allow assessors to give appropriate credit to levels of performance in the key areas of designing, constructing and testing, as well as allowing assessors to differentiate between different levels of performance. This has improved the internal verification process as well as overall performance. In addition, opportunities exist to share experiences and provide support through social media, as well as regional networking.

Previously, some centres had difficulty getting staff with the relevant experience to deliver, assess and internally verify the National 5 Practical Electronics course. This has significantly improved, with more experienced staff now delivering the course. This is reflected in the number of centres with ‘accepted’ or ‘accepted*’ outcomes, which is encouraging.

Lots of good assessment and verification practices was evident during visits. For example, most centres documented how they had made final assessment judgements, resulting in a high level of consistency. In most cases, centres provided useful and effective feedback to candidates, as shown in the assessment records.

Useful resources

- National 5 Practical Electronics — practical activity case study: good practice (this resource highlights good practice from candidates and centres)
- National 5 Practical Electronics — Practical Electronics audio presentations (this resource covers each stage of the practical activity and supports the assessor’s interpretation and application of the marking instructions)