NQ Practical Electronics Qualification Verification Summary Report 2024–25

Section 1: verification group information

Verification group name:	Practical Electronics
Verification activity:	Visiting
Round:	2
Date published:	July 2025

National Course components verified

Course code	Course level	Course title
C860 75	National 5	Practical Electronics practical activity

Section 2: comments on assessment

Assessment approaches

There was a range of practical activity tasks available for centres to select from, and all were similar in complexity. Regardless of the task chosen, or the experience of the assessor, candidates performed well at certain elements and found other elements challenging. In all tasks the challenging elements were creating circuit layout diagrams,

creating test plans and final circuit analysis. The more practical, less reflective tasks such as circuit simulation and construction were done reasonably well by candidates.

All aspects of each available task provided sufficient opportunity for candidates to demonstrate different levels of performance, from analysis and design through to build test and final reporting.

The marking instructions, supported by available Understanding Standards support materials, allowed assessors to give appropriate credit to key levels of performance in all key areas of design, build and test as well as allowing assessors to differentiate between different levels of performance in all key areas of design, build and test.

The marking instructions functioned as expected as all the centre's marks were within tolerance after a revisit to one centre. Where a centre had an 'accepted*' this was usually due to inexperience with the industrial aspects of electronics such as clarity of layout diagrams and conventions used (colour coding of layout wires), soldering and interconnection techniques for circuit boards, test planning and resulting. If candidates struggle to produce a strip-board layout, the assessor should provide a fully annotated solution to use for circuit construction.

Centres should also ensure that that they have a range of suitable tools, consumables and other resources so that candidates can maximise marks for the practical aspects of the course.

The following points were noted from visits with regard to assessment approaches:

- Candidates were given the opportunity to complete all sections of the design brief, construction and report using their own methods. Candidates were given adequate time to complete the design, construction and to report on the project. Candidates were given an appropriate level of support throughout the practical activity which was reflected in the assessor marking and cross marking from internal verifier. Application of the marking instructions was evident and the general outline was conveyed to give candidates a full understanding of the standards required to complete the practical activity.

- Candidates that struggled with analysis and design were marked accordingly but given working solutions in order to progress to the more practical elements.
- Some centres would benefit from access to consumables that allow the insertion of fixed test points at circuit nodes that tie into candidate test plans. This would support candidates to take measurements to enhance the enactment of their test plans and support them in enacting possible repairs.
- In the component list task, centres could consider skill builder tasks for this area, by having candidates complete costing exercises on earlier circuits in preparation for this task. Testing worked effectively when candidates had identified areas to test earlier on in their simulation work. This is an area to develop in future years.

Assessment judgements

Overall, the practical activity met the standard as most deviations were within tolerance. Most deviations were due to the experience of the assessor in delivering the course and applying the marking scheme. However, the marking scheme is robust enough to ensure that deviations in marks given were within tolerance.

Where a centre had an ‘accepted*’, this was usually due to inexperience with the industrial aspects of electronics such as clarity of layout diagrams and conventions used (colour coding of layout wires), soldering and interconnection techniques for circuit boards, test planning and resulting. Layout diagrams should include all interconnections and track cuts. Layout diagrams should be created using the actual footprint of each component and not the simulation circuit symbol.

The actual circuits built should replicate the layout diagrams to ensure consistency, but it may be necessary to make changes, for example axial capacitors may become radial capacitors due to component ordering.

Professional circuit labelling kits can be purchased so that candidates will not need to use a marker pen to label stripboards. The colour of the wiring used should reflect industrial practice and not just what is available.

The following points were noted from visits with regard to assessment judgements:

- The majority of marks, for most candidates, were gained with the practical elements of the course. Assessors marked candidates in line with the course requirements and had detailed and comprehensive marking spreadsheets for each candidate detailing all marks allocated.
- As circuits are constructed each board should be checked for accuracy and candidates given suitable feedback to ensure that they can improve marks for the later circuits.
- There was leniency when assessing ‘Detailed component layout diagrams’. For some candidates, there were no track breaks or breaks were in the wrong place.
- All the candidates sampled did not follow the correct convention for wiring. All of them used green wires in the process subsystem constructed; one candidate also used white wires. For ‘Neatness of subsystem layout’, candidates should also be assessed on the correct convention of colour codes. For example, pin 14 should be connected to the +Vs rail with a red wire; pin 7 should be connected to the 0 V rail with a black wire.
- Test points should be planned and included in the layout diagram.

The majority of the candidates sampled had difficulties with similar areas such as system or block diagram, application of test pins and the subsequent circuit testing.

Section 3: general comments

As expected, the more experienced assessors were able to guide candidates to a better performance. However, there is a wealth of support available to all assessors to tap into if they wish. There is also a strong support network for assessors and internal verifiers using social media.